Semiconductors and integrated circuits

Part 6b August 1979

ICs for digital systems in radio and television receivers

SEMICONDUCTORS AND INTEGRATED CIRCUITS

PART 6b - AUGUST 1979

ICs FOR DIGITAL SYSTEMS IN RADIO AND TELEVISION RECEIVERS

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of three series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS AND INTEGRATED CIRCUITS	RED
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

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October 1977

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Part 7	September 1971	CM7 09-71	**Circuit blocks** Circuit blocks 100 kHz-series, circuit blocks 1-series, circuit blocks 10-series, circuit blocks for ferrite core memory drive
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Part 8	June 1979	CM8 06-79	**Variable mains transformers**
Part 9	August 1979	CM9 08-79	**Piezoelectric quartz devices** Quartz crystal units, temperature compensated crystal oscillators
Part 10	April 1978	CM10 04-78	**Connectors**

FUNCTIONAL AND NUMERICAL INDEX

SELECTION GUIDE BY FUNCTION

REMOTE CONTROL SYSTEMS

For general purpose application

SAF1032P	receiver/decoder for infrared operation
SAF1039P	remote transmitter for infrared operation

For simple and middle class TV receivers

SAA5000	remote control transmitter encoder
SAA5010	remote control receiver decoder
SAA5012A	remote control receiver decoder

For sophisticated radio and television systems

SAB3011	remote transmitter
SAB3012	receiver and analogue memory
SAB3022	receiver and analogue memory
SAB3032	receiver and analogue memory
SAB3042	infrared decoder; microcomputer compatible
TDB1033	preamplifier for ultrasonic/infrared remote control transmission

DIGITAL CHANNEL SELECT SYSTEM (DICS OR TRD)

Control systems

SAB2021	instruction encoder
SAB3011	remote transmitter
SAB3012	receiver and analogue memory
SAB3017	IBUS sub-system interface
SAB3022	receiver and analogue memory
SAB3032	receiver and analogue memory
TDB1033	preamplifier for ultrasonic/infrared remote control transmission

Tuning systems

SAB1009B	wide-band limiting amplifier
SAB1046	1 GHz divider-by-256
SAB2015	control and station memory circuit
SAB2022	fine detuning circuit
SAB2024	frequency control circuit
SAB2034	frequency control circuit for Italian TV channels

Display systems

SAB1016	control circuit for on-screen display of station and/or channel number

VIDEO TUNING SYSTEMS (VTS)

Control systems

SAB3011	remote transmitter
SAB3042	infrared decoder; microcomputer compatible
TDB1033	preamplifier for ultrasonic/infrared remote control transmission

Tuning systems

SAB1009B	wide-band limiting amplifier
SAB1046	1 GHz divider-by-256
SAB3013	6-function analogue memory; microcomputer controlled
SAB3024	computer interface for tuning systems
SAB3034	analogue and tuning circuit

Display systems

SAA1060	LED display/interface circuit

TELETEXT AND VIEWDATA

Teletext decoder ICs

SAA5020	Teletext timing chain circuit
SAA5030	Teletext video processor
SAA5040	Teletext acquisition and control circuit
SAA5041	Teletext acquisition and control circuit
SAA5043	Teletext acquisition and control circuit
SAA5050	Teletext character generator (English)
SAA5051	Teletext character generator (German)
SAA5052	Teletext character generator (Swedish)

RADIO TUNING SYSTEMS

SAA1056	PLL frequency synthesizer
SAA1058	125 MHz amplifier and divider-by-32/33
SAA1060	LED display/interface circuit
SAA1062	LCD display/interface circuit

FREQUENCY MEASUREMENT AND DISPLAY SYSTEM

SAA1058	125 MHz amplifier and divider-by-32/33
SAA1070	display interface and frequency counter

NUMERICAL INDEX

GENERAL

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

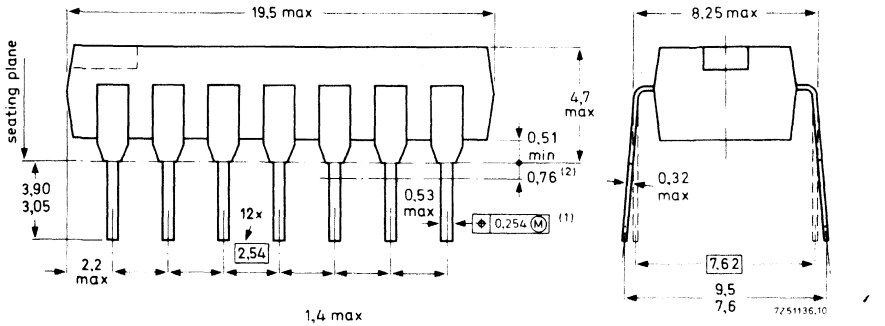
To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

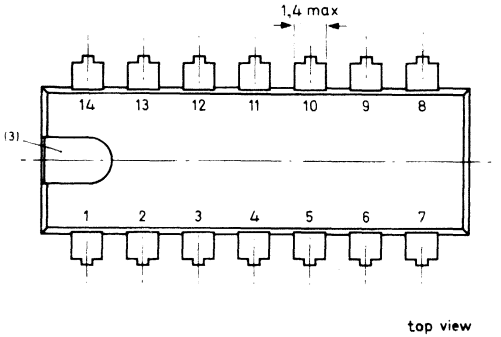
Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

PACKAGE OUTLINES

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27S, T, V)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

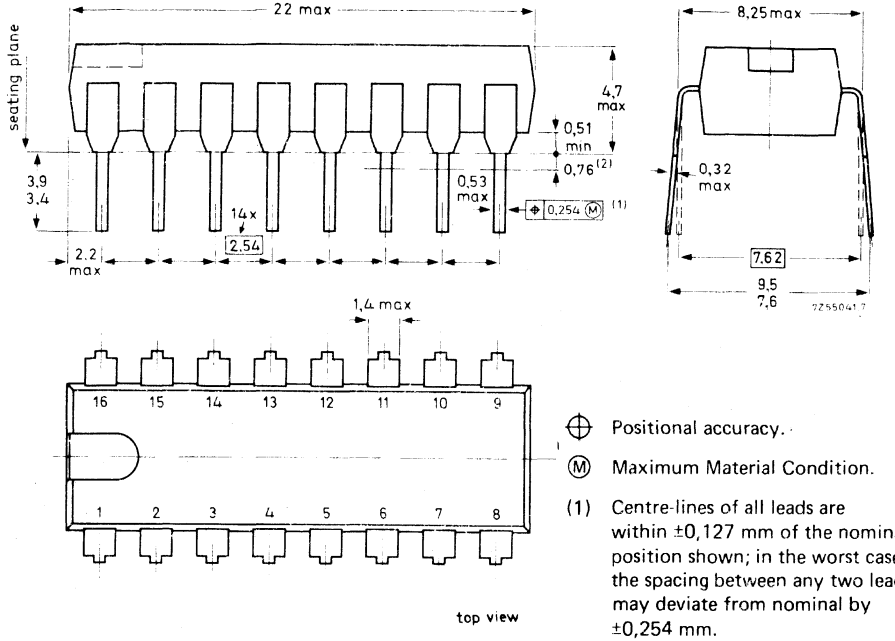
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
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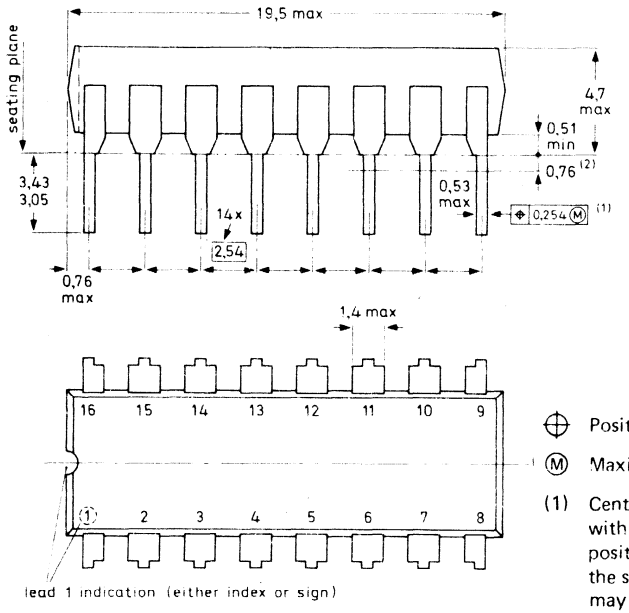
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

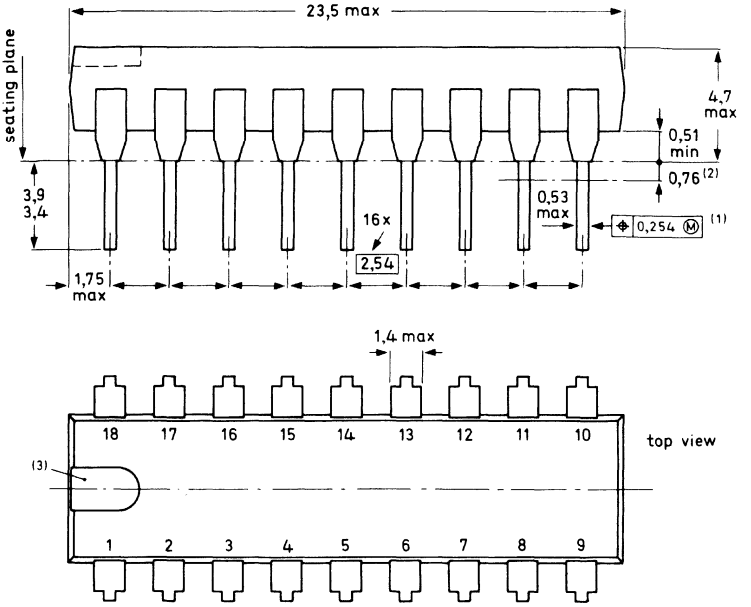
2. By dip or wave

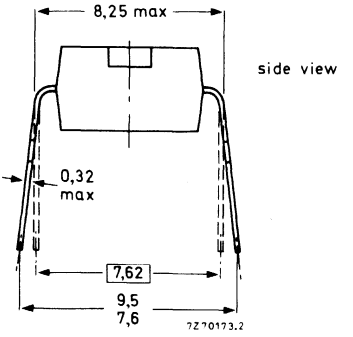
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

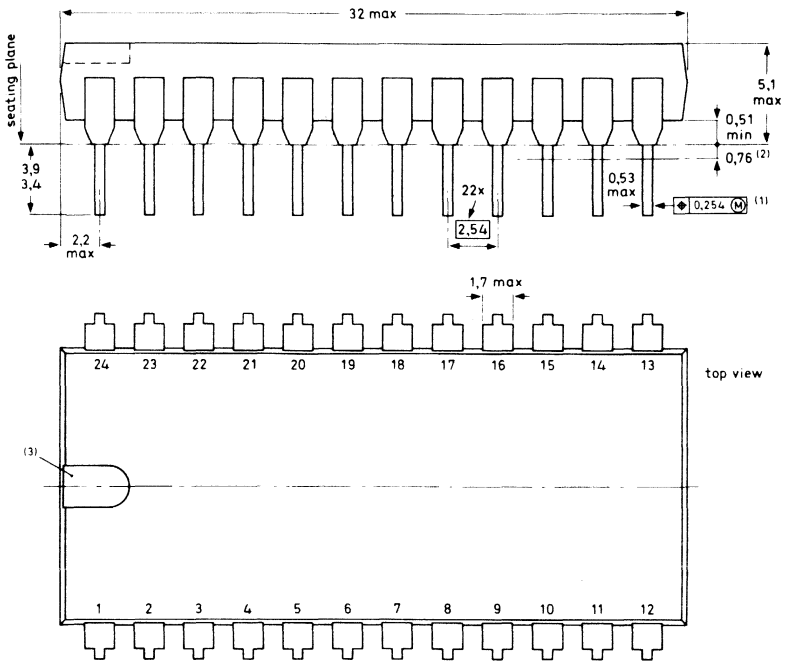
(3) Index may be horizontal as shown, or vertical.

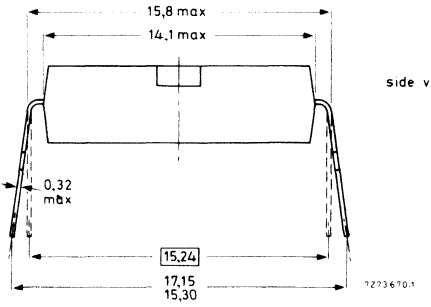
Dimensions in mm

SOLDERING

See page 1 of this chapter (SOT-27S, T, V)

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

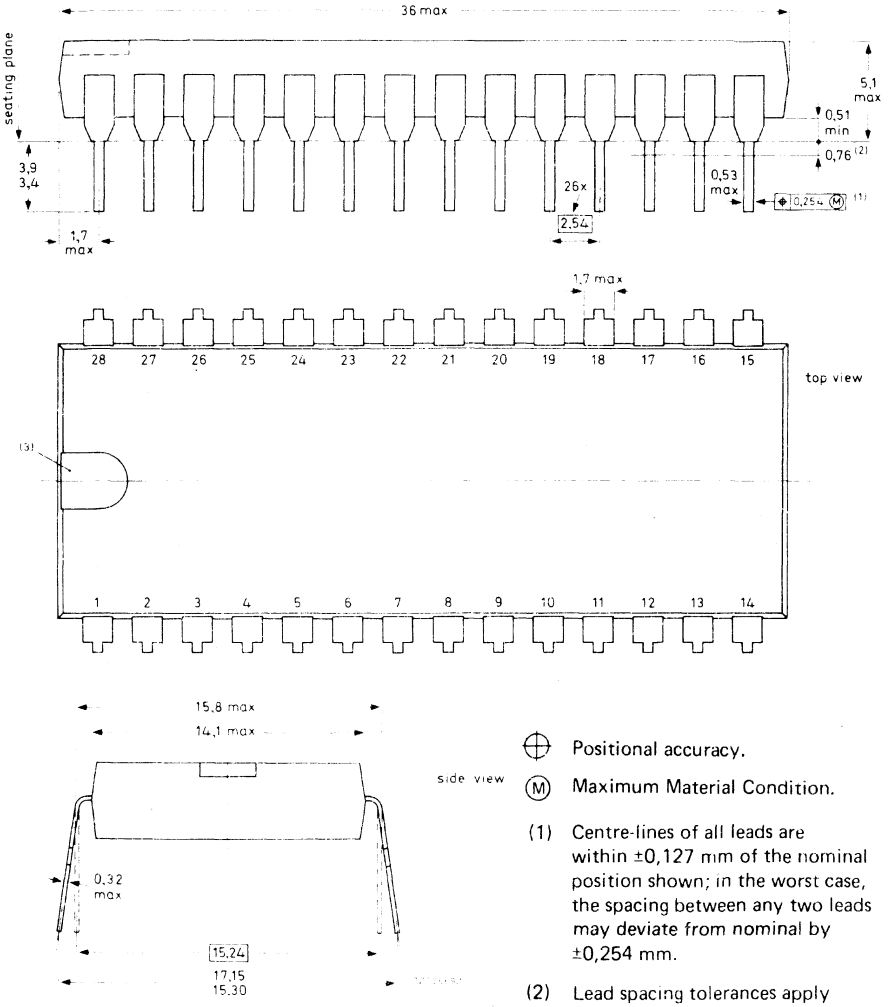
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See page 1 of this chapter (SOT-27S, T, V)

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

SOLDERING

See page 1 of this chapter (SOT-27S, T, V)

INTRODUCTION TO DIGITAL SYSTEMS

TUNING AND CONTROL SYSTEMS FOR RADIO AND TV RECEIVERS, TEXT DECODERS AND TV GAMES

FOREWORD

TV and radio receivers have conventionally used analogue tuning and control systems. However, the development of LSI technology has now progressed to the state where these functions can be economically performed by mass-produced digital LSI circuits. Bulky and unreliable multi-way switches and potentiometers can be replaced by simple single-pole switches. Moreover, the digital circuitry allows the use of remote control systems, again developed using LSI techniques.

New functions for the TV receiver, such as Teletext and video games, can easily be accommodated using digital control techniques. This handbook describes a complete range of LSI circuits designed to perform all tuning, control and remote control functions required for TV and radio receivers. The processes used to fabricate these ICs vary according to the function, for example, ECL for high-frequency circuits, LOCMOS for low-power circuits, etc. However, all circuits are produced by basically simple processes, providing good yield and reliability.

Available systems

- Remote control systems: three different remote control systems are available which cope with different market or system requirements.
- DICS (Digital Channel Select) system (also referred to as the TRD system): the well-known system in volume production; closed loop digital tuning, based on the FLL (frequency locked loop) principle; including remote control and display features.
- VTS (Video Tuning System): the next generation system for microcomputer based closed loop tuning systems (FLL principle); a full range of microcomputer peripherals.
- Teletext and Viewdata systems: the new digital text communication systems with on-screen text display.
- RTS (Radio Tuning System): digital tuning, control and display system for radio receivers, with or without remote control.
- Digital Frequency Counter system: frequency measurement and display system for radio receivers.

The systems are designed so that they can be operated independently or built into a single system. Their compatible design philosophy means that basic systems can easily be expanded when design requirements are changed. Moreover, the TV and radio systems can be operated independently via a single remote control unit, while sub-systems such as TV games, slide and film projectors and recorders can be operated via the TV or radio equipment. Figure 1 shows a typical system approach, controlling TV, radio etc. from a single transmitter unit.

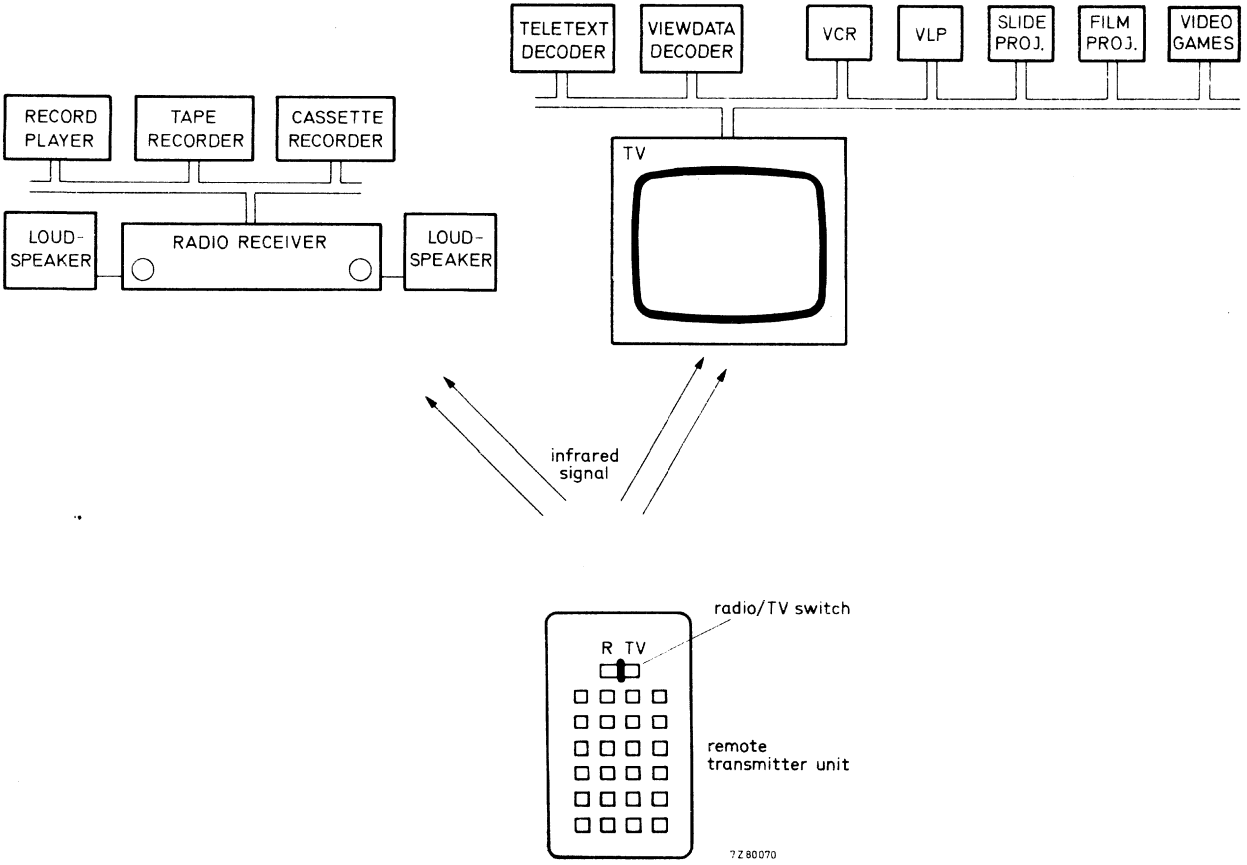


Fig. 1 Control of a radio and a TV reception system with dependent sub-systems by means of remote control.

SURVEY OF REMOTE CONTROL SYSTEMS

Three different remote control systems are offered to suit the different requirements.

- SAF1032; SAF1039: the simple and cheap remote control system with 3 analogue functions and 32 commands.
- SAA5000; SAA5010 family: 32 commands and 4 analogue functions, specially designed for optimum co-operation with touch control ICs and the Teletext decoder circuits.
- SAB3011; SAB3012 family: the most sophisticated system with 2 x 64 commands for radio and TV applications; to this family belong the SAB3022, SAB3032 and SAB3042.

SURVEY OF THE DICS system (TRD)

This is a remote control and digital tuning system intended primarily for use in TV receivers; provision has been made, however, for using the remote control with radio receivers and other sub-systems. The system incorporates a memory for station storage and analogue settings.

Control system

The control system comprises:

- SAB3011 remote transmitter;
- SAB3012, SAB3022 or SAB3032 receiver and analogue memory circuits;
- TDB1033 signal amplifier;
- SAB2021 command encoder (local use);
- SAB3017 serial to parallel command translator.

Tuning system

- SAB2024 frequency comparator and ROM;
- SAB2015 control circuit and RAM (station storage);
- SAB1009B + SAB1046 input amplifier and frequency divider (prescaler). This combination will be superseded by the SAB1018 one chip prescaler;
- SAB2022 analogue memory for fine de-tuning.

Display system

- SAB1016 control circuit for on-screen display of station and/or channel number.

Features of the DICS system are:

Tuning

- Highly accurate tuning allows optimum reception of Teletext;
- AFC compensates for drift in frequency converters, VCRs or TV games;
- Fully automatic direct digital selection and tuning of all current and future TV channels in the VHF and UHF range, including those outside the standard tuning range;
- Stable closed-loop tuning system with an error of less than 10 kHz;
- Simple storage of preferred-station frequencies;
- Fine de-tuning of stored station according to personal preference;
- Non-volatile station storage;
- Fast search tuning;
- Search tuning will also locate stations outside the normal channel pattern.

Control

- Large command set of 2 groups of 64 commands allows operation of two receiver systems from one transmitter, e.g. TV and radio;
- 8 sub-systems selectable per command group, leaving 56 commands for each sub-system (Teletext, Viewdata, TV games etc.);
- Transmitter modulation method provides reliable error-free reception of commands;
- 31 local commands directly available, expandable up to 64.

Display

- Transmitter identified by display of channel and station numbers by on-screen display;
- On-screen display uses character rounding and background blanking.

Brief functional description

Figure 2 shows the layout of a typical DICS system. The SAB3011 remote transmitter generates a serial command code when a command key is depressed. The code is transmitted using infrared or ultrasonic radiation, using a modulation technique that eliminates the effects of background or interference radiation.

The receiver and analogue memory (REAM) demodulates the serial command word and waits until two identical, consecutive commands have been received before passing the command to the rest of the system, via the IBUS. Analogue function commands are obeyed inside the REAM to provide the required analogue outputs.

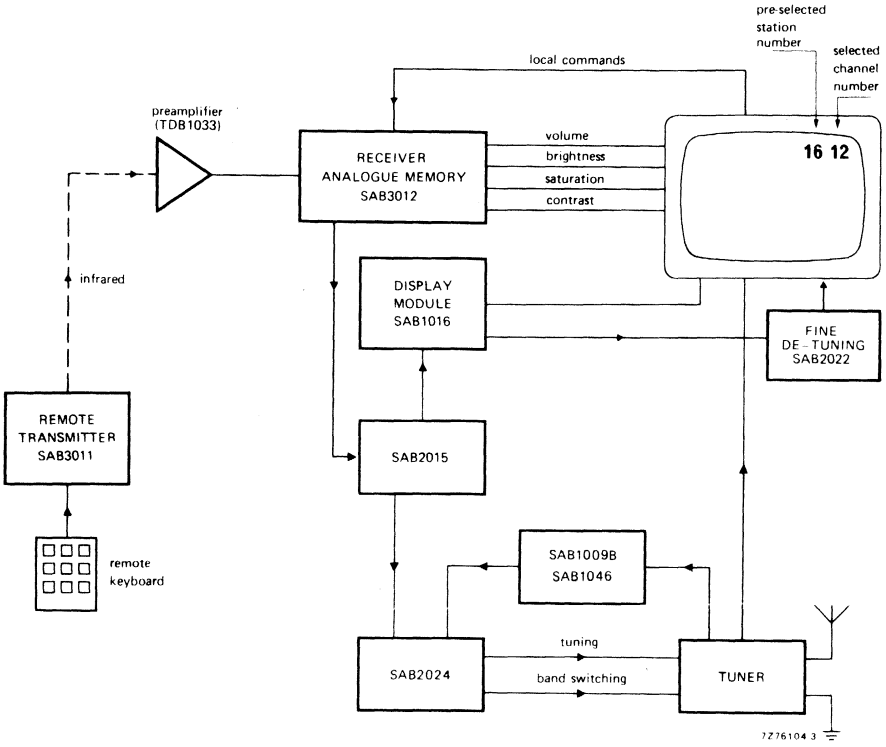


Fig. 2 Layout of a typical DICS system.

The digital tuning section comprises the channel selector, an input amplifier and frequency divider, and a frequency comparator with ROM. The ROM is used to store all the standard CCIR-allocated TV carrier frequencies. The output of the frequency comparator drives the AFC circuit to lock the tuner to the desired frequency. After reception of a tuning command, the ROM is addressed by the required channel number (from the SAB2015) to load the control loop with the frequency information for the required station. This information is also used to provide station and channel numbers for display purposes. These numbers can be presented as an on-screen display using the SAB1016.

The fine de-tuning circuit, SAB2022, delivers an offset voltage for the IF/AFC module. The de-tuning voltage can be set to one of 32 levels for each of the 16 stored stations.

The SAB2021 can be used to generate the serial IBUS commands from a local keyboard matrix. Figure 3 shows the SAB2021 in an application requiring local control only.

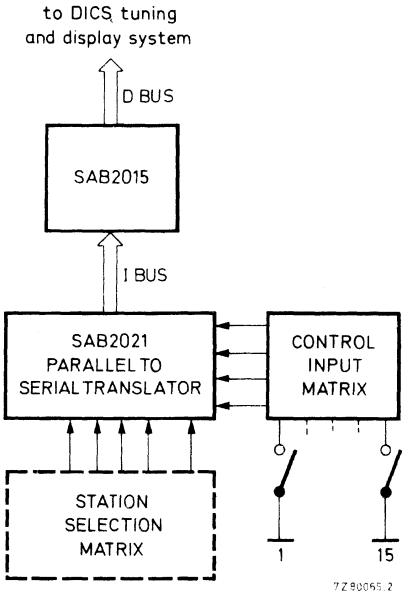


Fig. 3 Circuit SAB2021 providing local command inputs.

SURVEY OF THE VTS SYSTEM (Video Tuning System)

The VTS system is the successor of the DICS concept, using the same tuning principles and remote control transmitter SAB3011, but is based on microcomputer control rather than on dedicated circuits, to guarantee optimum design flexibility. It is possible to realize very economic concepts by using a simple microcomputer such as the 8021. If more features are required, more sophisticated systems can be designed by using the 8048 or even the 8049 microcomputers.
An attractive feature of our concepts is, that the tuning part of these different systems is the same.
The following circuits can be used:

Control

SAB3011	remote transmitter for 128 commands.
SAB3042	remote control decoder for 128 commands with an asynchronous bus to the microcomputer; an IBUS to videotex circuits, e.g. Teletext and Viewdata. Inputs for local keyboard (31 mask-programmable commands possible).
TDB1033	signal amplifier.

Tuning system

SAB3024	computer interface for tuning systems; this is a microcomputer peripheral for tuning.
SAB3034	analogue and tuning circuit; a microcomputer peripheral for tuning and 6 analogue functions.
SAB3013	computer controlled analogue memory providing 6 analogue functions.

Display

SAB3016	(in development) for microcomputer controlled on-screen display.
SAA1060	control and drive circuit for LED display of station and channel numbers.
SAA1061	control and drive circuit for LED display of station and channel numbers.

Typical applications

The basic VTS

Figure 4 shows a simple low-cost VTS which is based on an 8021 microcomputer and is suitable for incorporation in the more basic type of television receivers which are often without a.f.c. circuits. The basic system performs the following functions:

- Direct access to all CCIR channels by entering two digits on the local keyboard.
- Stepping sequentially through the channels in one or both directions.
- Search tuning in one or both directions.
- LED display of channel number.
- No a.f.c. required.

The basic system can be extended as follows:

- Remote control can be added by connecting the TDB1033 amplifier directly to the microcomputer, and using the infrared transmitter SAB3011.
- The computer-controlled analogue memory SAB3013 can be added to provide fine detuning, control of five analogue functions (e.g. volume, brightness, contrast, saturation and tone), muting and setting of all the analogue levels to mid-value at switch-on. If the receiver has a.f.c. it is possible to reduce the cost of the system by using the SAB3034, which performs the dual functions of tuning and analogue control, instead of the SAB3024 and SAB3013.
- A non-volatile memory (MNOS or CMOS with battery back-up) can be added to provide preset station facilities and set the analogue levels to user-selected values at switch-on.

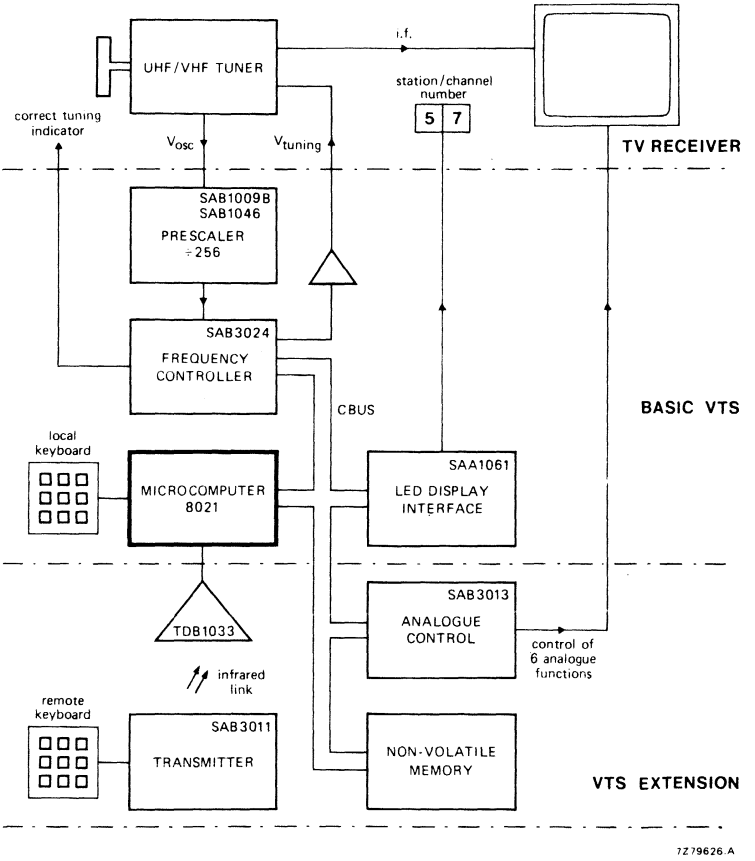


Fig. 4 A basic VTS system with extension for station memory, analogue function control and remote control.

A VTS for middle-class receivers

Figure 5 shows a more complex remotely-controlled VTS which is based on an 8048 microcomputer and is intended for incorporation in middle class television receivers. The system performs the following functions:

- Direct access to all CCIR channels.
- 20 or more preset stations (dependent on memory capacity).
- Stepping sequentially through the channels in one or both directions.
- Search tuning in one or both directions.
- Selection of channels and stations by decimal key entry.
- Local and remote control.
- Fine detuning with storage of detuning information.
- Control of five other analogue functions with muting.
- Setting of analogue levels to user-selected values at switch-on.
- On-screen display of station and channel number.

The system can be extended as follows:

- Addition of SAB3042 simplifies the task of the microcomputer and allows straightforward interfacing with videotex circuits (e.g. Teletext and Viewdata).
- The LED display interface SAA1061 can be used instead of, or in addition to, the on-screen display IC SAB3016.
- The frequency and analogue function controller SAB3034 can be replaced with the frequency controller SAB3024 and the analogue function controller SAB3013. The system could then be used in television receivers without a.f.c.

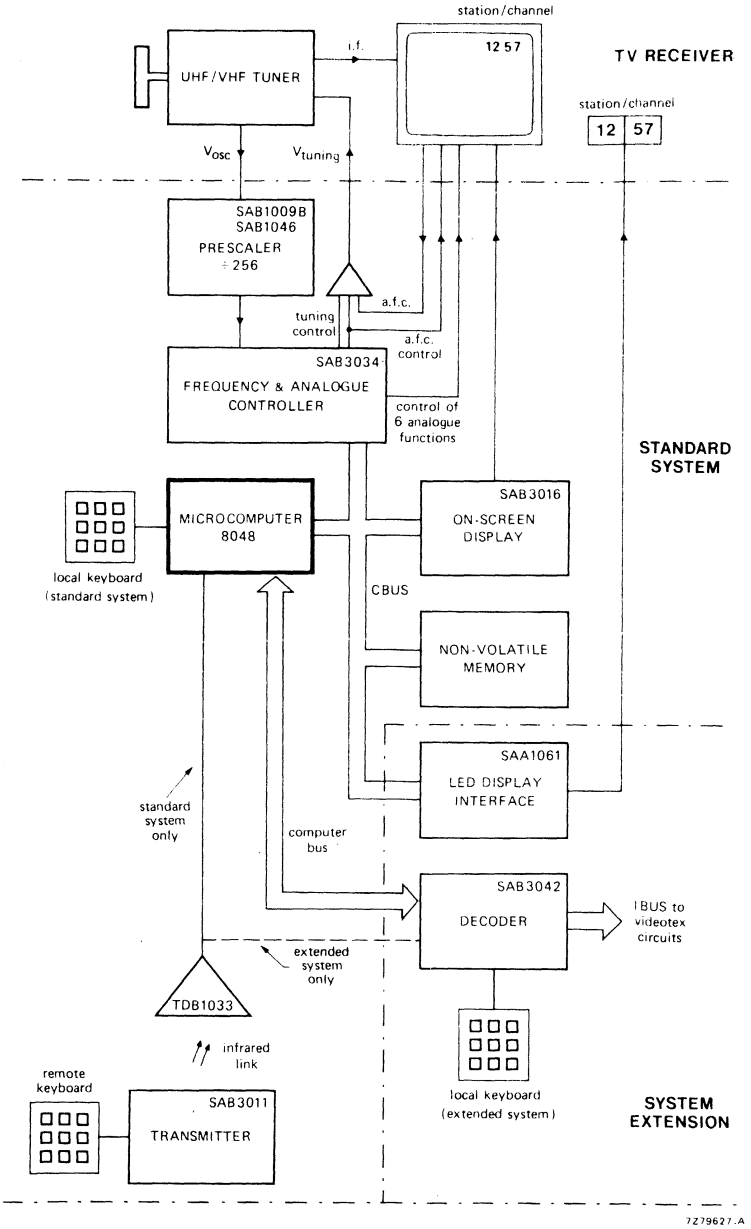


Fig. 5 A VTS system for middle class receivers.

A fully comprehensive VTS

Figure 6 shows a fully comprehensive VTS which is based on an 8049 microcomputer and is intended for incorporation in top-class television receivers. The system incorporates all the facilities provided by the system shown in Fig. 5 with the following additions:

- A timer/clock circuit.
- On-screen display of station/channel number or time of day.
- LED display of station/channel number or time of day.
- If control of videotex circuits is not required, an integrated circuit for character and graphic displays could be added. A video display IC for this purpose is being developed.

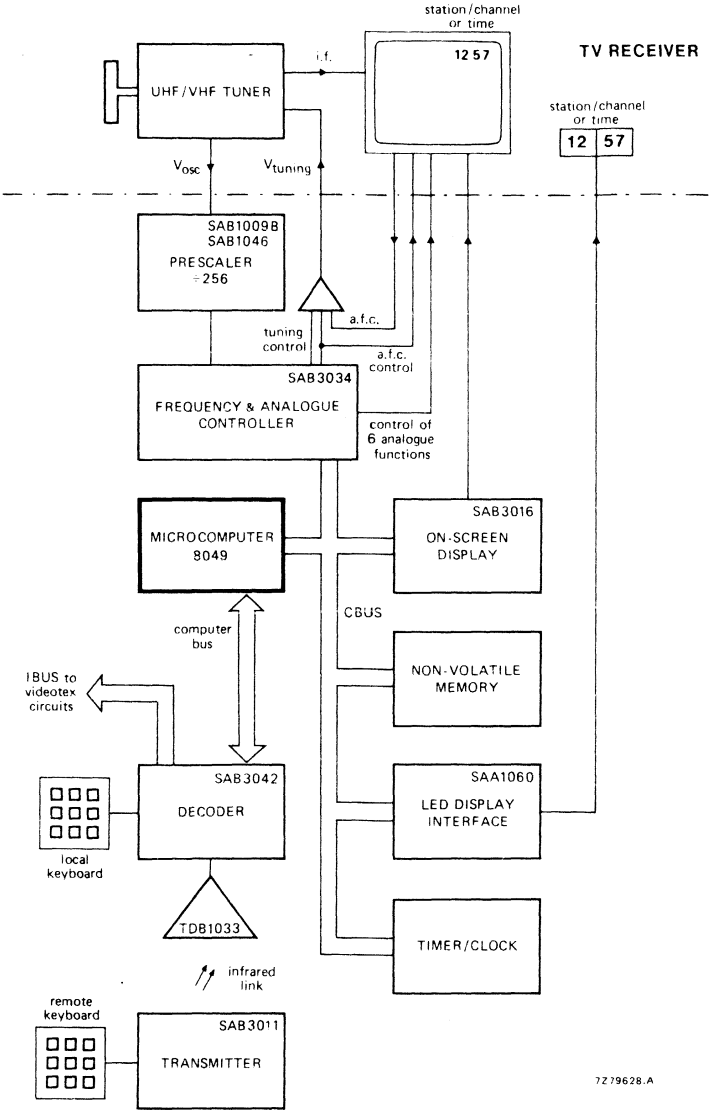


Fig. 6 A fully comprehensive VTS system.

TELETEXT AND VIEWDATA

Teletext

Teletext is a system whereby additional information is broadcast within the composite TV signal to provide information display upon the TV screen. With the necessary decoding circuits in the receiver, 'pages' of text can be displayed in place of, or superimposed upon, the transmitted picture.

Teletext information is transmitted during the vertical flyback blanking period of the TV signal. The Teletext decoding circuits process and store this information until the complete required page is available, when it is displayed on the screen. Existing services divide the information into magazines, each containing up to 100 pages. A page consists of 24 rows of 40 alphanumeric characters.

The Teletext decoder can be operated by the remote control system SAB3011 and SAB3012. An alternative remote control system, the SAA5000 and SAA5010, has been designed for the British market and provides optimum compatibility with Teletext and Viewdata decoders.

Features of the Teletext decoder

- Simple design using four LSI circuits;
- Simple operation by remote control;
- Can easily be extended to a Viewdata decoder;
- Crystal-controlled synchronization;
- Double height facility to double the character height and display half of a page;
- Character rounding improves readability;
- Messages can be superimposed on TV programme;
- Last page received can be displayed after transmitter shut-down;
- Preset timed operation possible.

Teletext transmission

Part of the vertical flyback time (return from lower right to upper left of the screen) is available for the transmission of Teletext. This corresponds to about 16 horizontal line periods. Figure 7 shows the timing of the Teletext data during the vertical blanking period. In this instance, Teletext information is transmitted during lines 17 and 18 for the first half-frame and during lines 330 and 331 for the second half-frame.

Teletext characters are transmitted in ASCII code (7-bit) with one parity bit to allow error detection in the receiver. The 7-bit code allows the use of up to 128 symbols and control codes. Hamming code is used while transmitting line addressing information so that errors in this can be corrected.

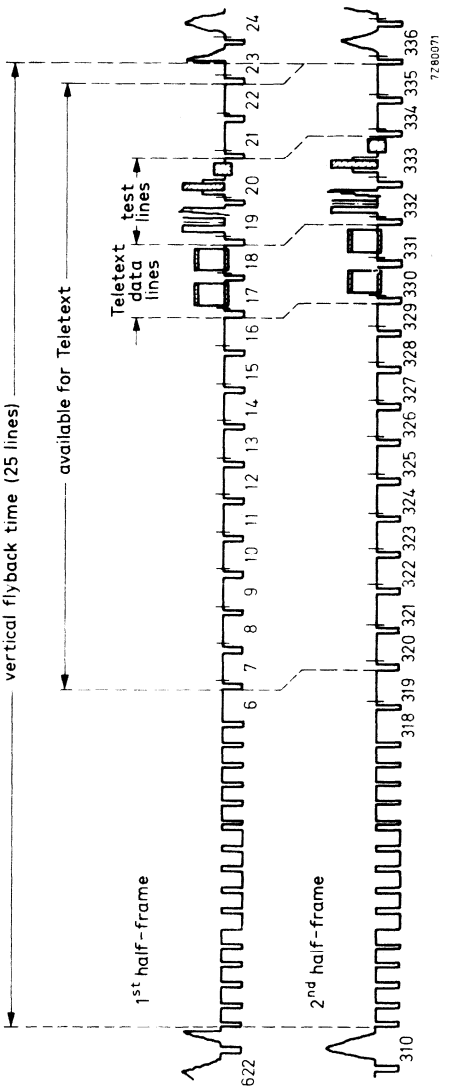


Fig. 7 Teletext data lines in the vertical blanking period.

Teletext decoder components

A range of LSI circuits has been developed to allow simple construction of a Teletext decoder. These dedicated LSI circuits perform the task of timing, video processing, control-and-data-acquisition, and character generation. The requirements of different markets have led to the development of alternative versions of the control-and-acquisition and character generator circuits. The page information store is comprised of standard RAM circuits.

Teletext decoder ICs:

- SAA5020 timing chain, providing the system timing;
- SAA5030 video input processor;
- SAA5040 (Britain)
- SAA5041 (Continent)
- SAA5043 (Australia)

  Teletext control-and-acquisition circuit;
- SAA5050 (English)
- SAA5051 (German)
- SAA5052 (Swedish)

  character generator.

The system also requires a static RAM of at least 1 K x 7-bit capacity.

Figure 8 shows a block diagram of the Teletext decoder and VTS system, with connections to a Viewdata system shown in broken lines. The text information is supplied to the receiver circuitry as conventional R, G and B signals together with blanking and synchronizing information.

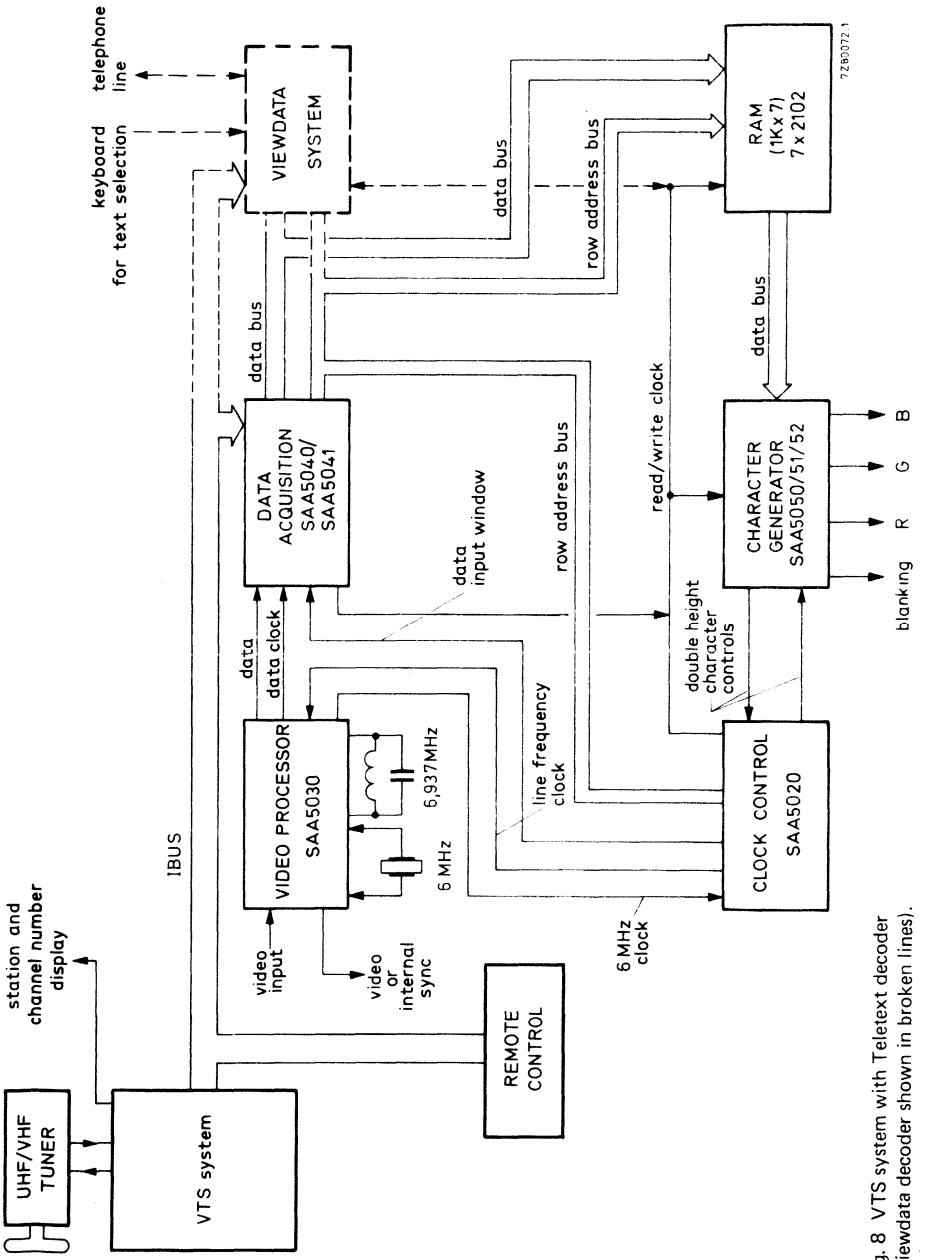


Fig. 8 VTS system with Teletext decoder (Viewdata decoder shown in broken lines).

Viewdata

Viewdata is an interactive data communication system, providing a two-way exchange of information. The information transfer takes place via a conventional telephone line and the information is displayed upon the TV screen. The conversational nature of the system means that it is not necessary to transfer all the available information, but only that requested. This means that vastly more pages can be made available and the capture time for any page can be reduced. The system does not depend upon the availability of a transmitted signal.

Figure 9 shows the schematic diagram of a Viewdata system. The video data is coded in the same manner as for Teletext, but is transmitted over the public telephone network. This results in low data transfer rates due to the limited bandwidth of the telephone system. Typical data rates are:

source to subscriber: 1200 baud;

subscriber to source: 75 baud.

Transmission of a complete page from source to subscriber takes about 8 s.

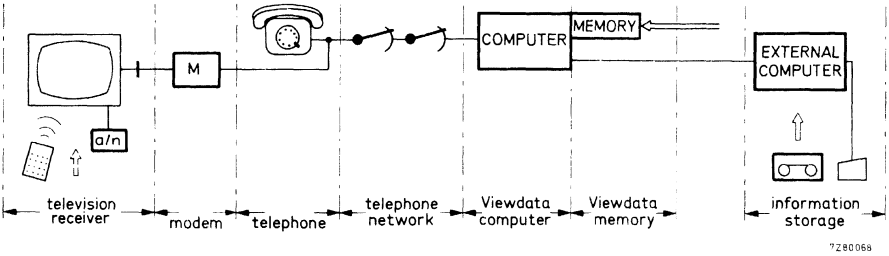


Fig. 9 The viewdata system.

The high storage capacity of Viewdata computer (typically 10^8 pages) means that the system can provide information on a vast range of subjects. Examples of this are: telephone directories; train, bus and airline time-tables; market quotations/prices; theatre, cinema and TV programmes etc. Furthermore, the system can be developed to provide communication between subscribers, replacing postal letters.

RADIO TUNING SYSTEM

- Crystal-controlled phase-locked-loop tuning system for high stability;
- LSI circuits designed for direct drive of displays and coupling to microcomputers;
- Connections to the SAA1056 and SAA1060 are minimized due to the controlled data format;
- Simple passive coupling to the tuner oscillator due to highly sensitive input of the SAA1058;
- Programmable reference frequency;
- Low radiation from the display driver due to the duplex operation mode;
- Few peripheral components are required.

Figure 10 shows a basic radio tuning system for AM and FM receivers. A microcomputer is used to provide a flexible interface between the user controls and the tuning and display sections.

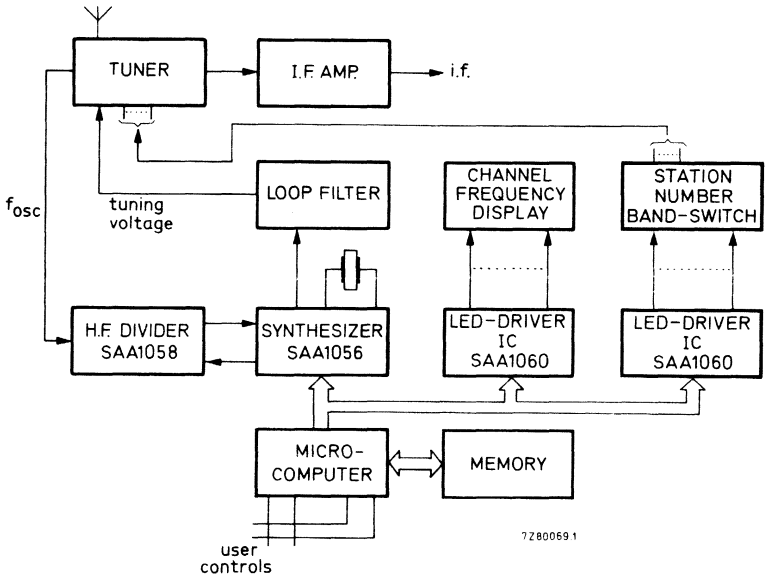


Fig. 10 A simple microcomputer-controlled radio tuning system.

Tuning section

- Tuner module;
- SAA1058 input preamplifier and divider;
- SAA1056 synthesizer module;
- Amplifier and loop-filter for the tuning voltage.

A phase-locked-loop is employed to maintain stable, accurate tuning. The oscillator output of the tuner is amplified and processed to become a square-wave which is passed to a frequency divider circuit with a programmable dividing factor. The output of the frequency divider is compared with a crystal-controlled reference frequency. The output of the comparator is amplified and filtered to be used as the tuner control voltage, providing a closed-loop control system. The user controls the system by keying-in a channel number or broadcast frequency, which is converted into the appropriate dividing factor by the microcomputer.

Additional features can easily be added to the system, such as search tuning, manual tuning and station memory.

Display section

The display section is driven from the serial data bus, its function being to display data such as frequency, channel number, station number, waveband etc. However, the design of the serial to parallel decoders allows control as well as display of general system functions and messages, such as:

- Volume, balance, bass or treble settings;
- Filter or mono/stereo switch positions;
- Unit status, such as cassette rewinding, recording or end-of-record.

Two special serial to parallel decoder ICs are available to drive LED or LCD displays from the serial data bus:

- SAA1060 16-bit serial to parallel decoder for 4½ digit drive in duplex mode;
- SAA1062 17 or 20-bit serial to parallel decoder for 17 or 20 segment drive.

Controls

The tuning system can be either locally or remotely controlled, or both. If the SAB3011 remote control system is used, the SAB3042 infrared decoder can be used instead of a REAM to provide a microcomputer-compatible output. A complete set of local controls can then be provided by an extra SAB3011. Figure 11 shows the radio tuning system with local and remote control and display facilities for various system functions.

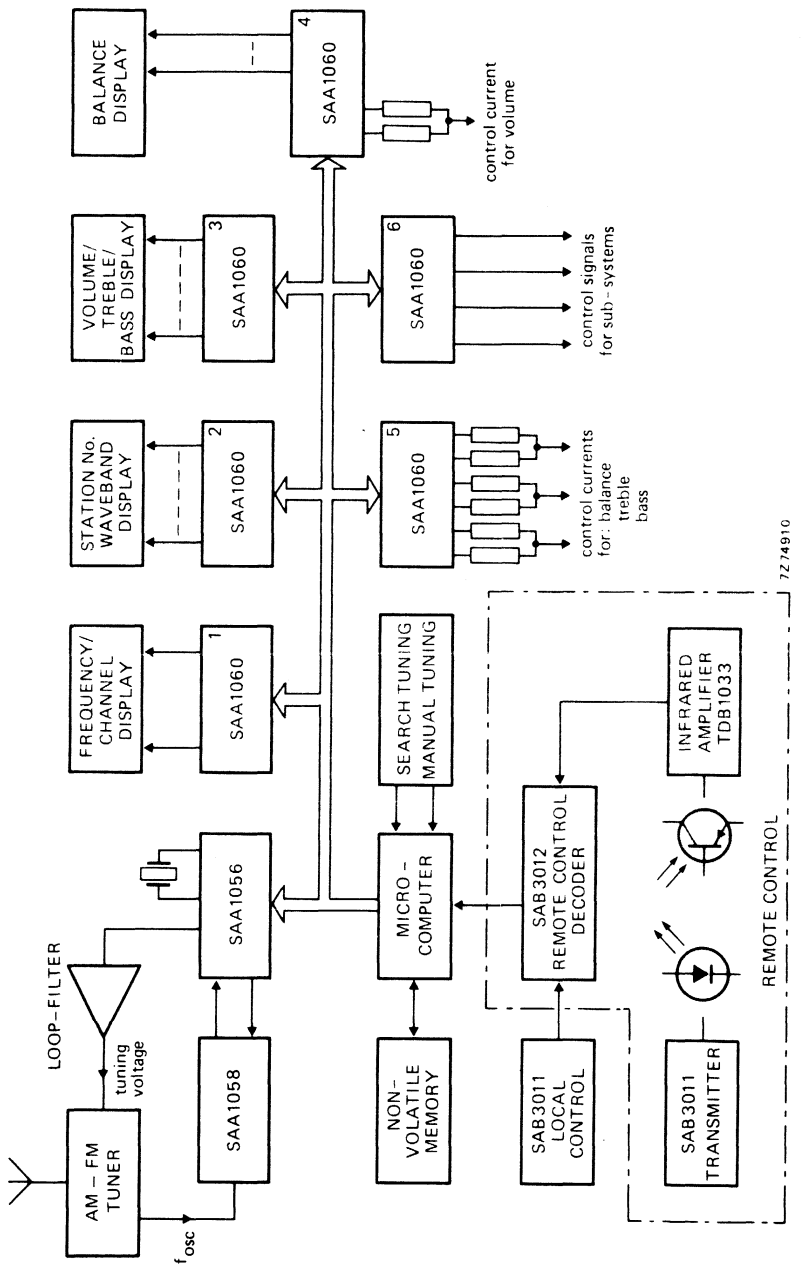


Fig. 11 Comprehensive radio receiver system employing the SAA1060 as display drive and D/A converters.

FREQUENCY MEASUREMENT AND DISPLAY SYSTEM

This system has been specifically designed to measure the frequency to which an a.m./f.m. radio is tuned and to provide a digital LED display of either the tuned frequency or the associated v.h.f. channel number.
The system is based on two ICs and can be used with v.h.f. (f.m.), short-wave, medium-wave and long-wave and can be programmed to compensate for a wide range of i.f. frequencies.

The following features are provided:

- Mains zero-crossing switching to reduce interference.
- Multiple sampling to stabilize display during short-term local oscillator drift.
- Requires only a single 8 V a.c. supply.
- Suitable for use with a wide range of i.f.:
  for a.m. 449 kHz to 472 kHz; for f.m. 10,6 MHz to 10,775 MHz.
- Compact circuitry with few peripheral components.
- Facilities for 'freezing', testing and blanking the display.
- Flicker suppression.
- High input sensitivity allows direct drive from radio local oscillators.

The principle of the frequency measuring and display system is illustrated by the block diagram in Fig. 12. The main components of the system are an integrated programmable prescaler (SAA1058), an integrated display interface and frequency counter (SAA1070), a 4 MHz quartz crystal and a 4½-digit seven-segment LED display.

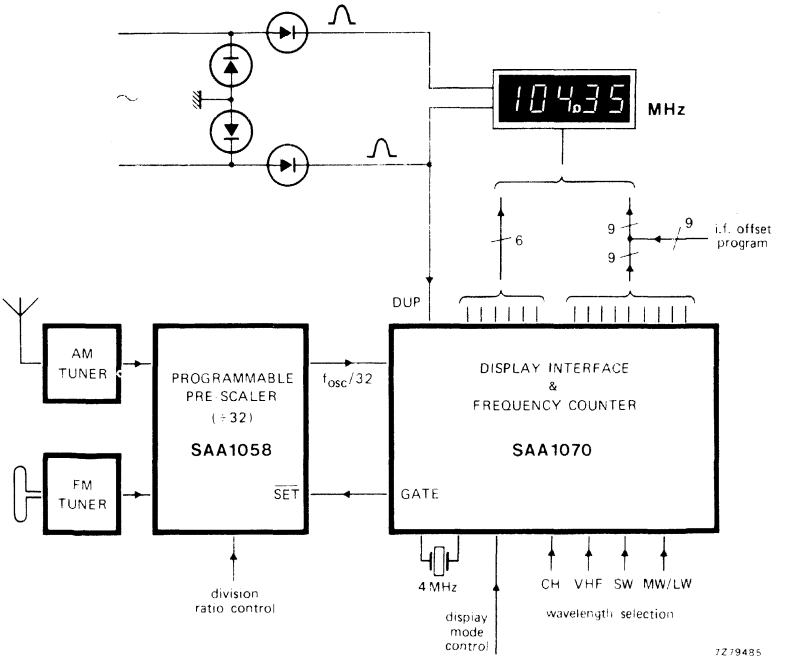


Fig. 12 Block diagram of a digital frequency indicator.

DEVICE DATA

PLL FREQUENCY SYNTHESIZER

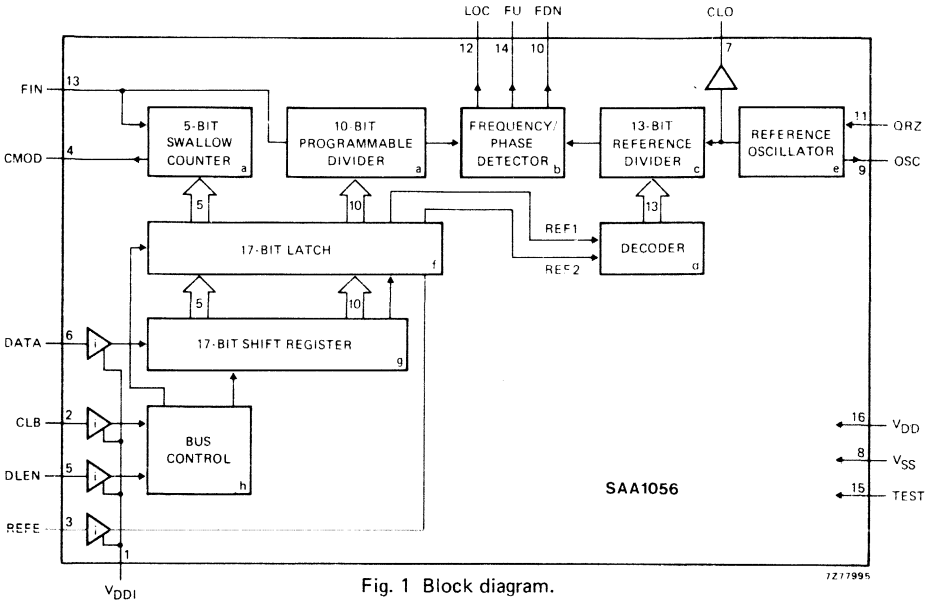


Fig. 1 Block diagram.

The integrated circuit SAA1056 together with a suitable prescaler (e.g. SAA1058) and a loop filter forms a complete PLL frequency synthesizer for AM/FM radio tuning systems.

Features

- Bus control for the selection of 16-bit words.
- 17-bit latch, for data storage.
- Control lines TTL compatible by means of level shifters.
- Decoupled oscillator frequency output (system clock for other ICs).
- Choice of 4 reference frequencies.

QUICK REFERENCE DATA

Supply voltage ranges	V_{DD}	8 to 10	V
	V_{DDI}	4,5 to 5,5	V
Operating ambient temperature range	T_{amb}	−20 to +80	°C
Input frequency	f_I	> 4	MHz

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

GENERAL DESCRIPTION

The integrated circuit SAA1056, together with a suitable prescaler (32/33) and loop-filter, forms a complete synthesizer function for AM/FM radio tuning systems.

The circuit comprises the following blocks:

a. A dividing circuit formed by a 5-bit binary Swallow counter with and a 10-bit binary programmable divider.
b. A frequency/phase detector which, via an external loop-filter, generates the control voltage for the voltage-controlled oscillator (VCO). The detector also gives a lock indication.
c. A 13-bit binary reference frequency divider. This divider delivers the reference frequency to the frequency/phase detector.
d. The decoder delivers the dividing number for the reference divider. Depending on the logic states of the 2 inputs (REF1 and REF2), four different dividing ratios (160, 400, 800 and 8000) for the reference frequencies can be fed to the frequency/phase detector.
e. A reference frequency oscillator. Together with a 4 MHz crystal a stable frequency is generated, from which the reference frequencies are derived. The 4 MHz signal is also available at a decoupled output as a system clock for other ICs.
f. A 17-bit latch to store the data for the dividing number of the programmable divider (block a) and 2 bits for reference frequency choice.
g. A 17-bit shift register to receive the serial data for the latch.
h. A bus control to avoid improper data to be handled by the system.
i. Level shifters for the control inputs DATA, DLEN, CLB and REFE so no external interface is necessary between the SAA1056 on 9 V and the other ICs on 5 V.

OPERATION DESCRIPTION

Data inputs (DLEN and DATA)

The SAA1056 accepts the serial 17-bit data word synchronized with the clock burst (CLB), are offered at the data input DATA. However, a command is accepted only when the data line enable input DLEN is HIGH at the same time.

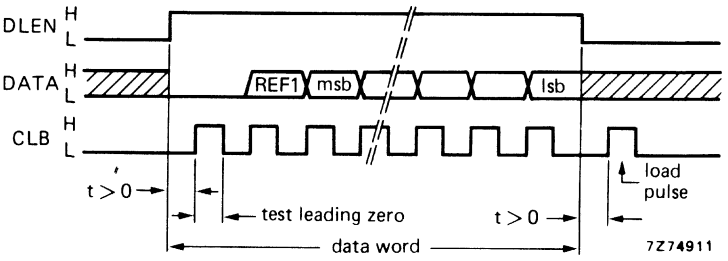


Fig. 2 Pulse diagram of the 17-bit data word.

Each data word must start with a leading zero. The SAA1056 checks the data word for the correct length (17 bits) including leading zero. The data word contains 15 bits as a binary coded ratio for the programmable divider. The first 10 bits program the 10-bit programmable divider and the next 5 bits program the Swallow counter (see Fig. 3). The 16th bit (REF1) determines the ratio of the reference divider in conjunction with the logic signal at input REFE.

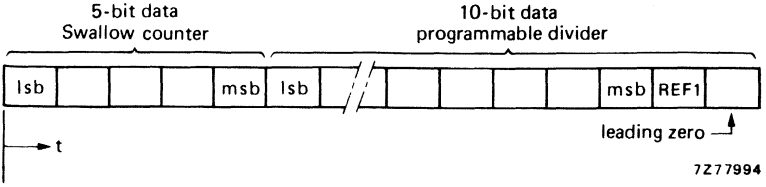


Fig. 3 Organization of a data word.

Setting the reference divider (input REFE and control-bit REF1)

The reference divider can be set to four different ratios, using the two signals REF2 and REF1:

control bit REF1	input REFE	dividing ratio N_{ref}	reference frequency at f_{osc} = 4 MHz; f_{ref}
1	1	160	25 kHz
1	0	400	10 kHz
0	1	800	5 kHz
0	0	8000	0,5 kHz

Input frequency divider (FIN)

The input frequency is applied to input FIN for further processing in the circuit. It is divided in the Swallow counter and the 10-bit programmable divider corresponding to the received data word. The dividing number of the dividing circuit is given by the following equation:

$N = N_S + P \times N_P$ with: $N_P \geqslant N_S$; $0 \leqslant N_S \leqslant 31$

in which:

N = dividing number of total divider
N_S = value for the Swallow counter
P = lowest dividing number of prescaler
N_P = dividing number of the 10-bit programmable divider.

OPERATION DESCRIPTION (continued)

In combination with the 32/33 divider (PRECO – SAA1058), the minimum and maximum dividing number can be calculated:

$N_{min} = 0 + 32 \times 31 = 992$
$N_{max} = 31 + 32 \times 1023 = 32\,767$

In combination with a standard 10/11 divider, the minimum and maximum dividing numbers are:

$N_{min} = 0 + 9 \times 10 = 90$
$N_{max} = 31 + 10 \times 1023 = 10\,261$

Count mode output for prescaler (CMOD)

Depending on the received data word, the 5-bit Swallow counter generates a signal for setting the prescaler.

0 = divide by low dividing number
1 = divide by high dividing number.

The signal appears about 150 ns after the input pulse FIN (see Fig. 4).

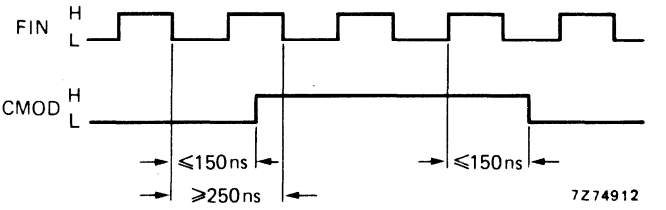


Fig. 4 Timing of the CMOD signal.

Phase detector (frequency up/down) and lock detector outputs (FDN, FU, LOC)

The frequency/phase detector outputs FDN and FU generate a control voltage via an external loop for the voltage-controlled oscillator (VCO).

FDN: phase detector output, frequency down
0 = active
1 = inactive

FU: phase detector output, frequency up
0 = inactive
1 = active

Output LOC generates an extra signal if the loop is locked.
0 = loop unlocked
1 = loop locked.

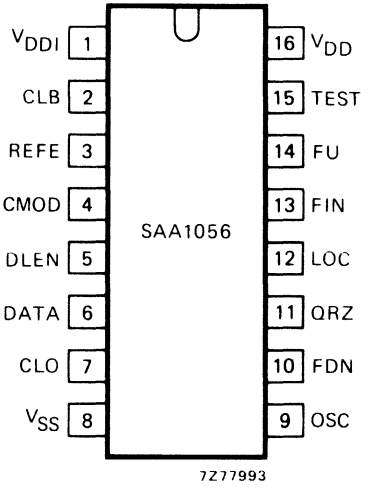


Fig. 5 Pinning diagram.

PINNING

16 V_{DD} positive supply
8 V_{SS} negative supply (0 V)

Inputs

1 V_{DDI} supply voltage for the level shifters
13 FIN input frequency; maximum 4 MHz
6 DATA data input for dividing numbers
2 CLB clock burst for data transmission
5 DLEN data line enable for data transmission
3 REFE reference frequency selection
11 QRZ quartz crystal input (4 MHz)

Outputs

4 CMOD count mode output for prescaler
12 LOC lock detector output
10 FDN phase detector output; frequency down
14 FU phase detector output; frequency up
7 CLO system clock for other ICs (4 MHz)
9 OSC quartz crystal oscillator output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to +11	V
Input voltage range	V_I	−0,3 to $+V_{DD}$	V
Input current	$\pm I_I$	max. 10	mA
Output current	$\pm I_O$	max. 10	mA
Current from V_{DDI} to V_{DD} ($V_{DDI} < V_{DD}$)	I	max. 10	mA
Power dissipation per output	P_O	max. 100	mW
Total power dissipation per package	P_{tot}	max. 300	mW
Operating ambient temperature range	T_{amb}	−20 to +80	°C
Storage temperature range	T_{stg}	−55 to +150	°C

CHARACTERISTICS

$V_{SS} = 0$; $T_{amb} = -20$ to +80 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltages	–	V_{DD}	8	9	10	V	
	–	V_{DDI}	4,5	5	5,5	V	
Quiescent current	10	I_{DD}	–	–	100	µA	$I_O = 0$; $V_I = V_{DD}$ or V_{DDI} or V_{SS}
Inputs without level shifters; FIN, QRZ, TEST							
input voltage LOW	8 to 10	V_{IL}	0	–	$0,3V_{DD}$	V	
input voltage HIGH	8 to 10	V_{IH}	$0,7V_{DD}$	–	V_{DD}	V	
input current HIGH	10	I_{IH}	–	–	1	µA	$V_I = 10$ V
input current LOW	10	$-I_{IL}$	–	–	1	µA	$V_I = 0$
input frequency	8 to 10	f_I	4	–	–	MHz	
duty factor	8 to 10	δ	45	–	55	%	
rise/fall time	8 to 10	t_r, t_f	–	–	50	ns	
Inputs with level shifters DATA, CLB, DLEN, REFE at V_{DDI} = 4,5 to 5,5 V							
input voltage LOW	8 to 10	V_{IL}	0	–	$0,2V_{DD}$	V	
input voltage HIGH	8 to 10	V_{IH}	$0,8V_{DDI}$	–	V_{DDI}	V	
input current HIGH	10	I_{IH}	–	–	1	µA	$V_I = 10$ V
input current LOW	10	$-I_{IL}$	–	–	1	µA	$V_I = 0$
rise/fall time	8 to 10	t_r, t_f	–	–	1	µs	
pulse width	–	t_{WH}, t_{WL}	500	–	–	ns	at 0,8 x V_{DD} resp. 0,2 x V_{DD} levels

	V_{DD} V	symbol	min.	typ.	max.		conditions
Outputs CMOD, CLO open-drain, n-channel							
output voltage LOW							
CMOD	8 to 10	V_{OL}	–	–	0,5	V	I_{OL} = 5 mA
CLO	8 to 10	V_{OL}	–	–	0,5	V	I_{OL} = 6 mA
output leakage current	10	I_{OR}	–	–	20	μA	V_O = 10 V
fall time; CMOD	8 to 10	t_f	–	–	20	ns	C_L = 25 pF; R_L = 1,2 kΩ ± 20%
fall time; CLO	8 to 10	t_f	–	–	50	ns	C_L = 50 pF; R_L = 1 kΩ ± 10%
Outputs LOC, FU, FDN							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}-0,5	–	–	V	$-I_O$ = 2,5 mA
output voltage LOW	8 to 10	V_{OL}	–	–	0,5	V	I_O = 5 mA
rise/fall time	8 to 10	t_r,t_f	–	–	20	ns	C_L = 25 pF; R_L = 10 kΩ ± 10%
Output OSC							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}-1	–	–	V	$-I_O$ = 1 mA
output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_O = 1,8 mA

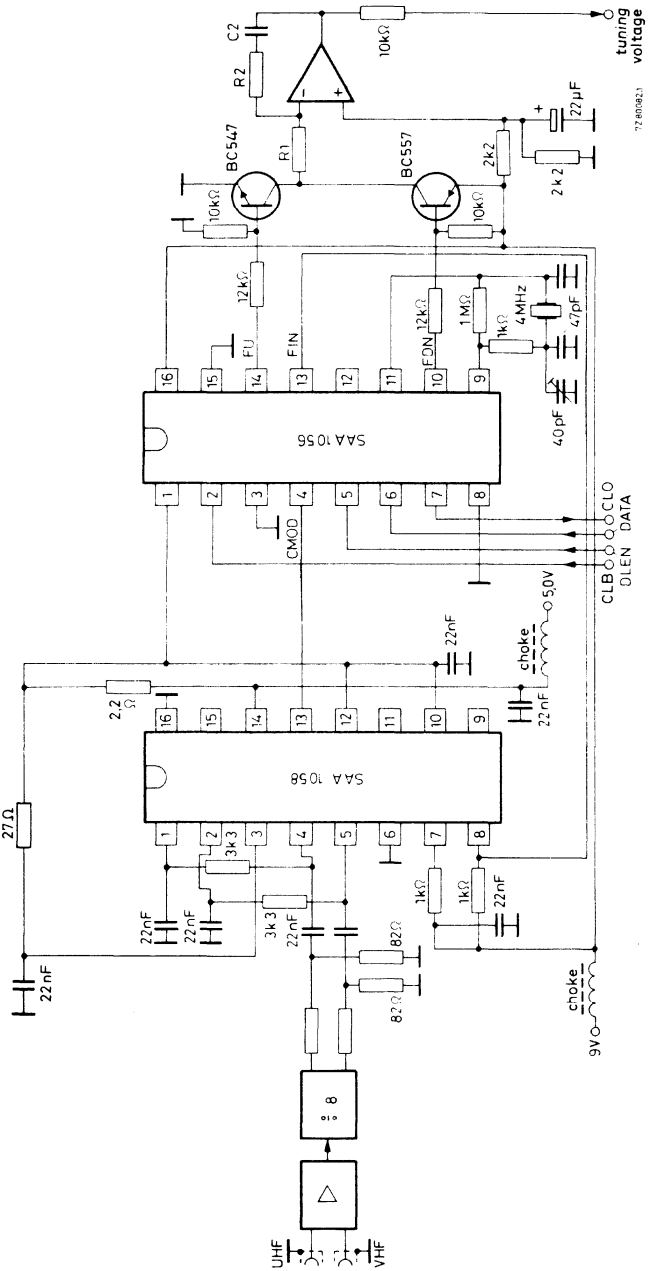


Fig. 6 Typical application of the SAA1056 with the SAA1058 in a TV receiver.

APPLICATION INFORMATION

DEVELOPMENT SAMPLE DATA

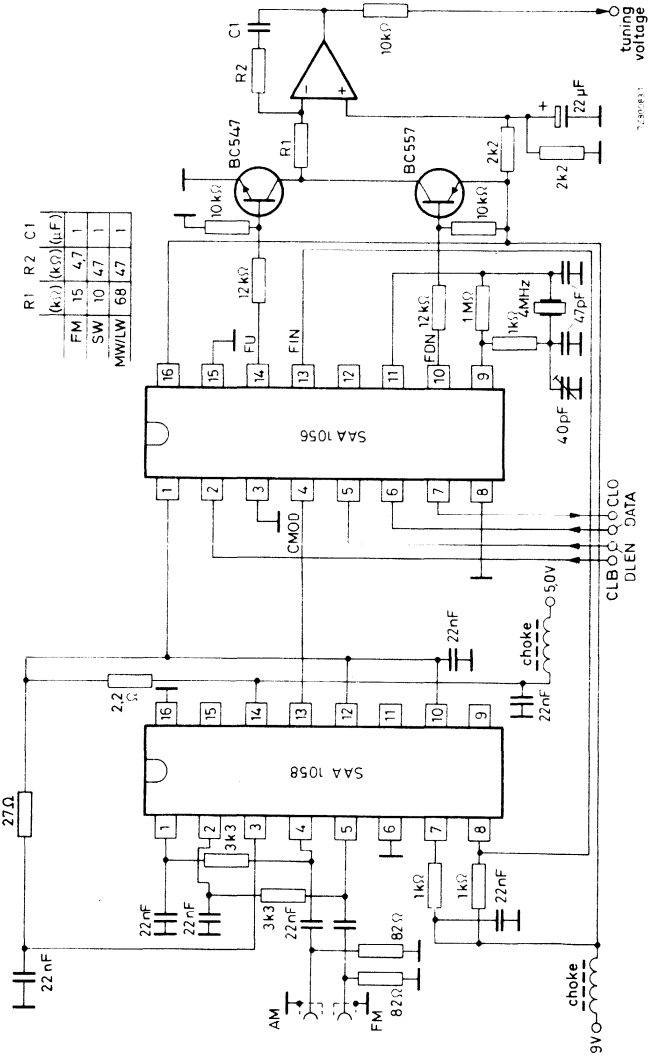


Fig. 7 Typical application of the SAA1056 with the SAA1058 in a radio receiver.

125 MHz AMPLIFIER AND DIVIDER-BY-32/33

The silicon monolithic integrated circuit SAA1058 is designed as a programmable-ratio divide-by-32/33 prescaler. It is intended for use in digital radio tuning systems and frequency counters in radio applications with an input frequency range from 0,5 to 125 MHz. The high-frequency inputs are differential inputs of a preamplifier for handling a.m. as well as f.m. oscillator signals. One output set provides complementary ECL levels by emitter followers and a second output buffer set is intended to drive MOS circuits by open collectors.

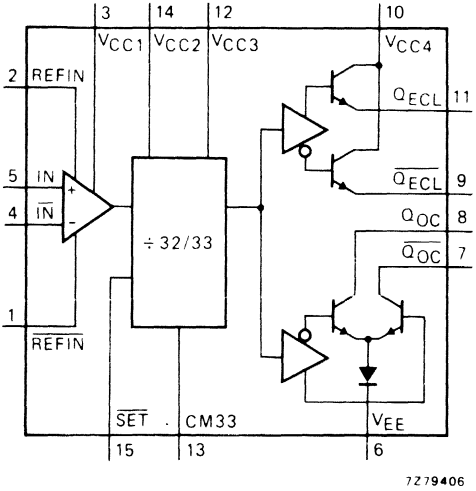


Fig. 1 Block diagram.

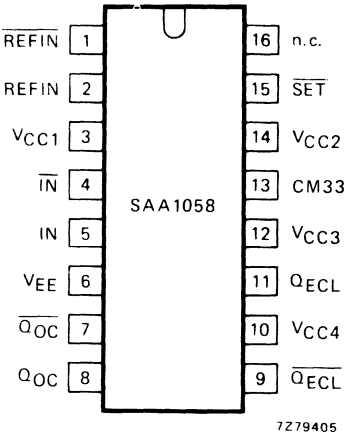


Fig. 2 Pin diagram.
$V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = 5$ V
$V_{EE} = 0$ V (ground)
Pin 16 preferably connected to V_{EE}

QUICK REFERENCE DATA

Supply voltage	V_{CC}		5 ± 10% V
Input frequency range	f_i		0,5 to 125 MHz
Input voltage range			
f = 0,5 to 30 MHz	$V_{i(rms)}$		5 to 100 mV
f = 30 to 125 MHz	$V_{i(rms)}$		10 to 100 mV
Power consumption per package (no load)	P_{av}	typ.	550 mW

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

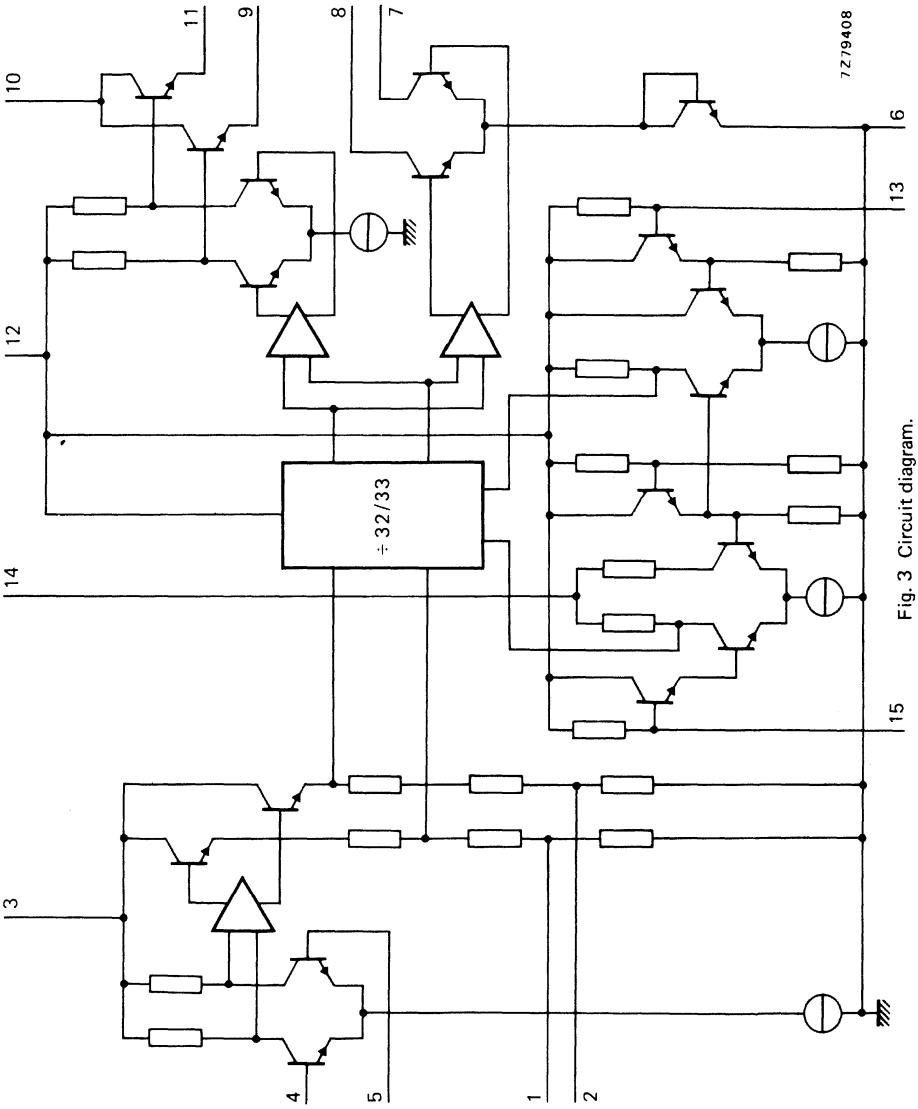


Fig. 3 Circuit diagram.

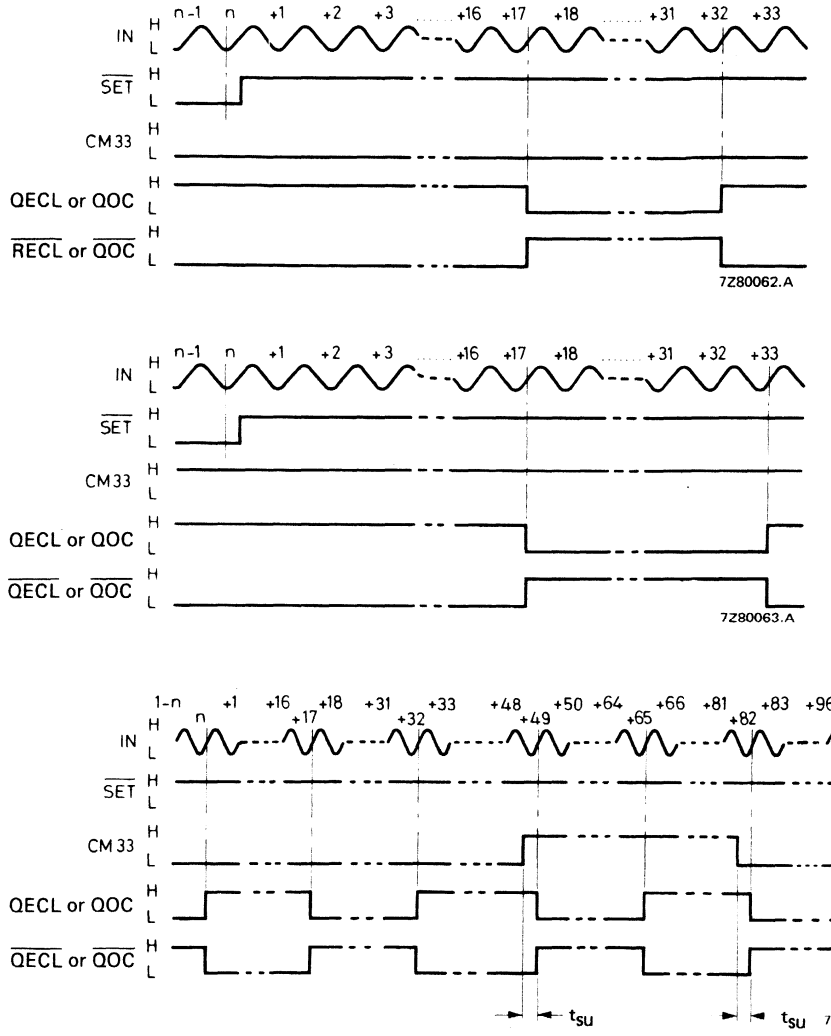


Fig. 4 Timing diagrams of programmable frequency dividing.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 3, 10, 12 and 14)	V_{CC}	max.	7 V
Output supply voltage (pins 7 and 8, R_L = 470 Ω)	V_{DD}	max.	14 V
Input voltage	V_I		0 to V_{CC}
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	0,76 W
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		−20 to + 60 °C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC} = 5 V (see Fig. 6); T_{amb} = 25 °C, unless otherwise specified.

Supply current ($I_3 + I_{10} + I_{12} + I_{14}$)*	I_{CC}	typ. <	110 mA 135 mA
Count input voltage (pins 4 and 5)			
A.M. (0,5 MHz to 30 MHz)	$V_{i(rms)}$		5 to 100 mV
F.M. (30 MHz to 125 MHz)	$V_{i(rms)}$		10 to 100 mV
A.C. input impedance	R_i	>	1 kΩ
Count mode input (pin 13)			
input voltage for division-ratio 32	V_{CML}	<	2 V
input voltage for division-ratio 33	V_{CMH}	>	3 V
input current at V_{CM} = 2 V	$-I_{CML}$	<	3,5 mA
Set-up time changing the division-ratio from 32 to 33 or vice versa	t_{su}	typ.	50 ns
Input capacitance	C_{CM}	typ.	1 pF
Reset input voltage (pin 15)			
reset	V_{RL}	<	2 V
no reset	V_{RH}	>	3 V
Input current at V_R = 2 V	$-I_{RL}$	<	2 mA
Emitter follower outputs (pins 9 and 11)			
output voltage; R_L = 4,7 kΩ to ground	V_{OH} V_{OL}	> <	3,7 V 3,3 V
Open collector outputs (pins 7 and 8)			
V_{DD} = 11 V; R_L = 470 Ω			
Output voltage HIGH	V_{OH}	>	9 V
Output voltage LOW	V_{OL}	<	2 V

* See Fig. 6.

CHARACTERISTICS (continued)

Open collector outputs (pins 7 and 8)
transition times, no capacitive load

t_{TLH}	typ.	15 ns
t_{THL}	typ.	12 ns

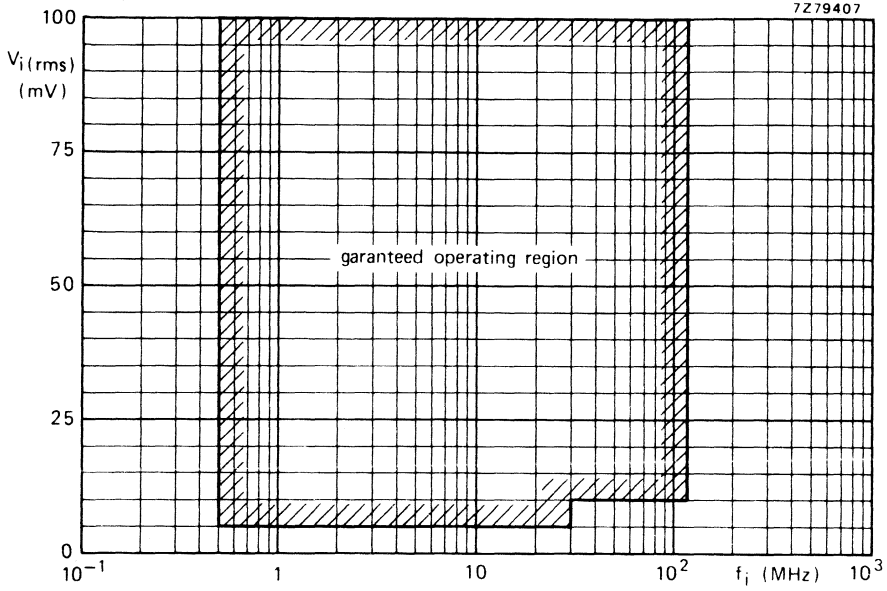


Fig. 5 Triggering level requirements.

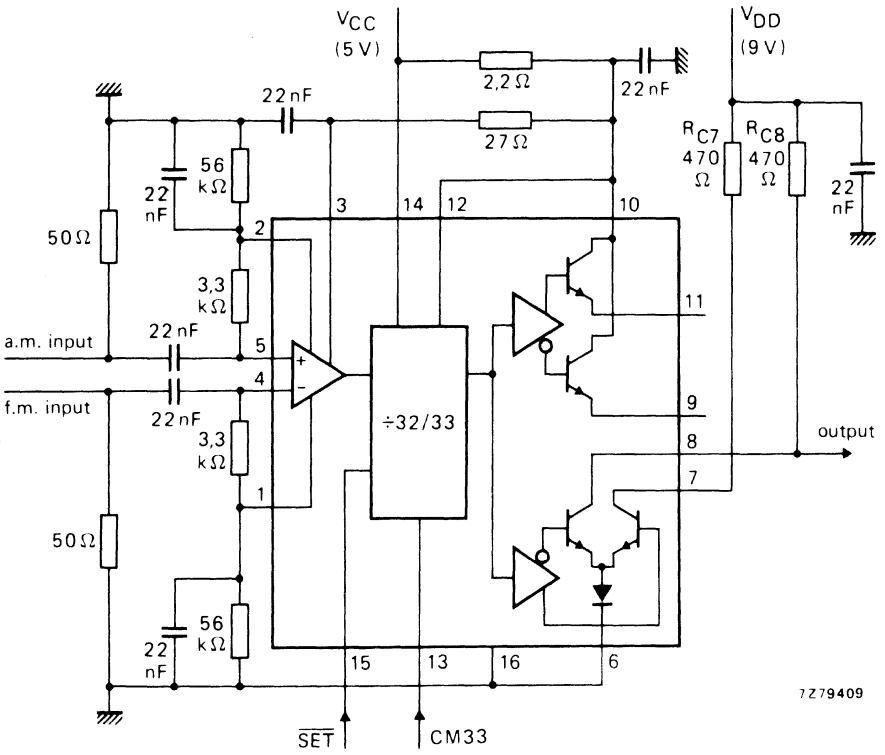


Fig. 6 Test circuit.

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION

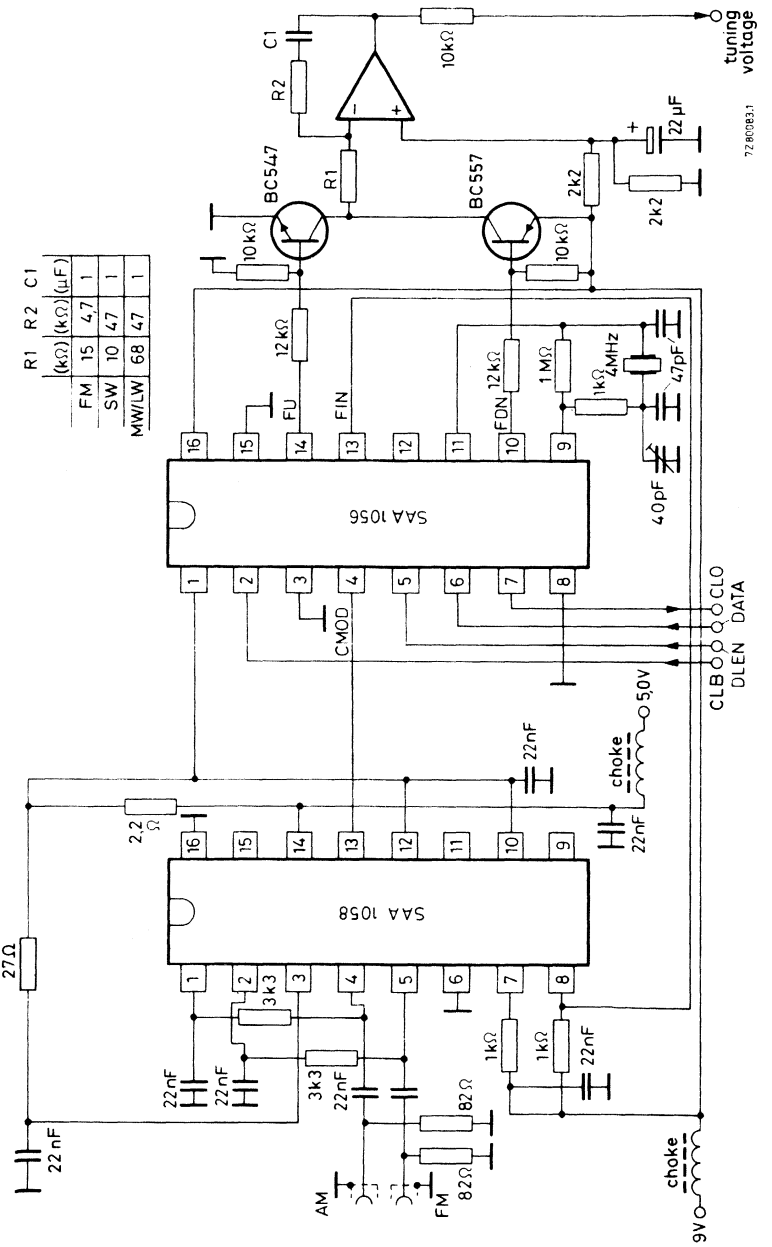


Fig. 7 Typical application of the SAA1056 with the SAA1058 in a radio receiver.

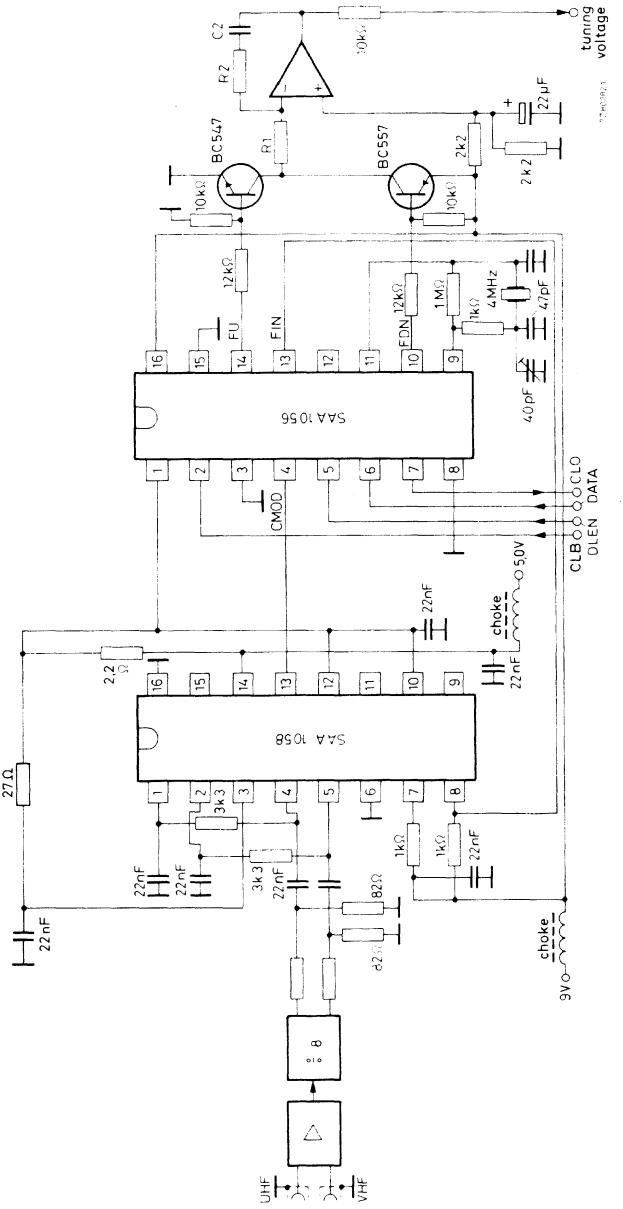


Fig. 8 Typical application of the SAA1056 with the SAA1058 in a TV receiver.

APPLICATION INFORMATION

LED DISPLAY/INTERFACE CIRCUIT

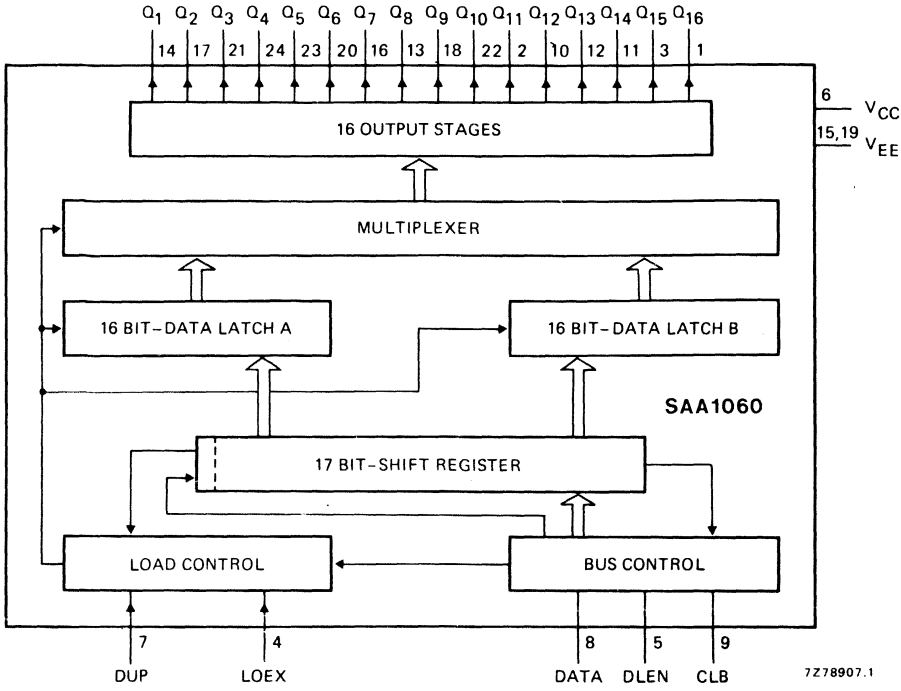


Fig. 1 Block diagram.

Features

- Driving 7, 14, 16-segment displays.
- Driving linear displays, bar graph displays for analogue functions.
- Serial to parallel decoder.
- Bus control for the selection of 18-bit words.
- 2 x 16-bit latch.
- Duplex operation for two modes of output: static (16 bit) or dynamic (2 x 16 bit).
- Data transfer control.
- 2 outputs for higher output current (80 mA).

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4 to 6 V
Operating ambient temperature range	T_{amb}		−20 to + 80 °C
Maximum input frequency	f_I	typ.	50 kHz
Supply current	I_{CC}	typ.	60 mA
Output current	I_Q	<	40 mA
Output current (Q_8 and Q_{16} only)	I_Q	<	80 mA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial to parallel decoder. Since the device has no decoder (this is handled by a microcomputer), it has many applications:

- driving 7-segment displays
- driving 14-segment displays
- driving linear displays, e.g. pointer, bar graph
- static output of switch-functions
- digital to analogue converter, with external R-2R network
- extension of the number of outputs for microprocessors or microcomputers.

Data transmission is initiated by means of a burst of clock pulses (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading zero. This allows different bus information to be supplied on the same bus lines for other circuits (e.g. SAA1056 with 16 bits).

The last bit (bit 17) of the data word contains the information which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are n-p-n transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs (Q_8 and Q_{16}) are arranged for double current, so that 2 x 2 segments can be connected in parallel.

OPERATION DESCRIPTION

Data inputs (DLEN, DATA)

The SAA1060 processes serially the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Fig. 3).

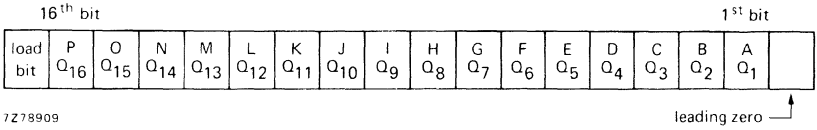


Fig. 2 Organization of a data word.

Condition for 17th bit:
0 = load data latch B
1 = load data latch A

The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

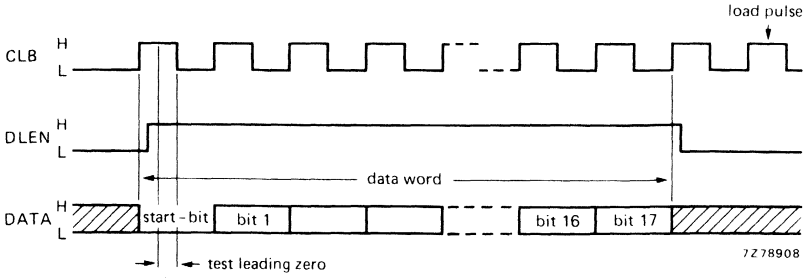


Fig. 3 Pulse diagram of the 16-bit data transmission.

Each data word must start with a leading zero. The SAA1060 checks the data word for the correct length (18 bits) and also for the leading zero.
The actual data is switched directly to the appropriate outputs. For switching on a segment, a '0' (LOW) is necessary at the appropriate data bit.

Data selection input (DUP)

The logic states at input DUP determine which of the two latch contents can be found on the output.

0 = latch A contents
1 = latch B contents

Load control input (LOEX)

Input LOEX determines the operation mode in which the device is able to work.

0 = duplex mode, i.e. output synchronized with the duplex signal
1 = d.c. mode, i.e. output direct from the by DUP selected data latch.

When operating in duplex mode at 50 Hz, the time between two data words to be transmitted must be > 21 ms.

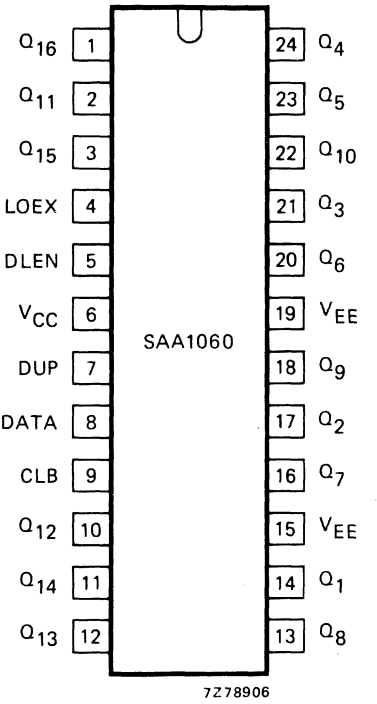


Fig. 4 Pinning diagram.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}	−0,3 to + 7	V
Total power dissipation	P_{tot}	max. 900	mW
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Storage temperature range	T_{stg}	−25 to + 125	°C

CHARACTERISTICS

V_{EE} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{CC} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{CC}	4	5	6	V	
Supply current	5	I_{CC}	–	60	–	mA	
Inputs DATA, CLB, DLEN, LOEX							
input voltage HIGH	5	V_{IH}	2	–	5	V	
input voltage LOW	5	V_{IL}	–	–	1	V	
input current LOW	5	$-I_{IL}$	–	–	20	μA	V_I = 0
maximum input frequency	5	f_I	–	50	–	kHz	
Input DUP							
input voltage HIGH	5	V_{IH}	0,8	–	12	V	
input voltage LOW	5	V_{IL}	−6	–	0,4	V	
input current HIGH	5	I_{IH}	0,01	–	12	mA	
maximum input frequency	5	f_I	–	50	–	kHz	
Outputs Q_1 to Q_7, Q_9 to Q_{15}							
output voltage HIGH	5	V_{OH}	–	–	16,8	V	I_{OH} = 0
output voltage LOW	5	V_{OL}	–	–	0,5	V	I_{OL} = 40 mA
output current LOW							
duplex mode	5	I_{OL}	–	–	60	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{OL}	–	20	40	mA	
Outputs Q_8 and Q_{16}							
output voltage HIGH	5	V_{OH}	–	–	16,8	V	I_{OH} = 0
output voltage LOW	5	V_{OL}	–	–	0,5	V	I_{OL} = 80 mA
output current LOW							
duplex mode	5	I_{OL}	–	–	120	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{OL}	–	40	80	mA	

LCD DISPLAY/INTERFACE CIRCUIT

Features

- Driving 7 to 20-segment displays.
- Driving linear displays.
- Serial to parallel decoder of digital signals.
- Bus control for the selection of 18/21-bit words.
- 17/20-bit latch.
- A.C. segment drive.
- On-chip oscillator.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	4,2 to 6	V
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Maximum input frequency	f_I	typ. 50	kHz
Supply current	I_{CC}	typ. 12	mA
Output current (Q_1 to Q_{20})	I_Q	> 60	mA

GENERAL DESCRIPTION

The SAA1062 is designed to drive a Liquid Crystal Display (LCD) of a digital tuning system. It contains a shift register with programmable length (18 or 21 bits), latches, both synchronized or static, exclusive-OR segment drivers (17 or 20 bits), an l.f. oscillator and a backplane driver for the LCD. The circuit is designed to be driven by a 3 bus structure from a microprocessor and can also be used as a programmable 17 or 20 bits serial-to-parallel decoder. It is also capable of storing 60 bits of information.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

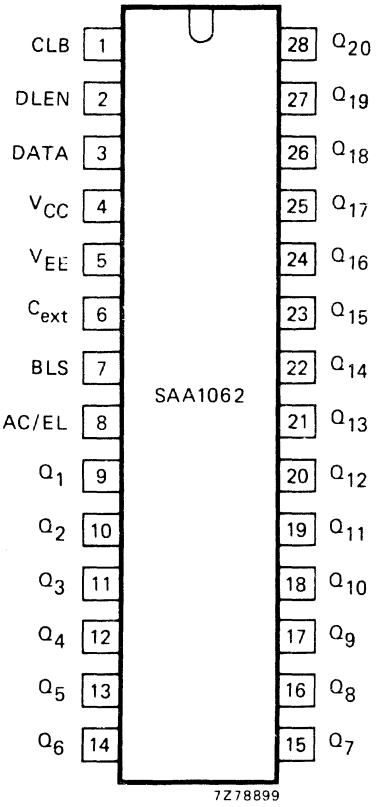


Fig. 1 Pinning diagram.

DEVELOPMENT SAMPLE DATA

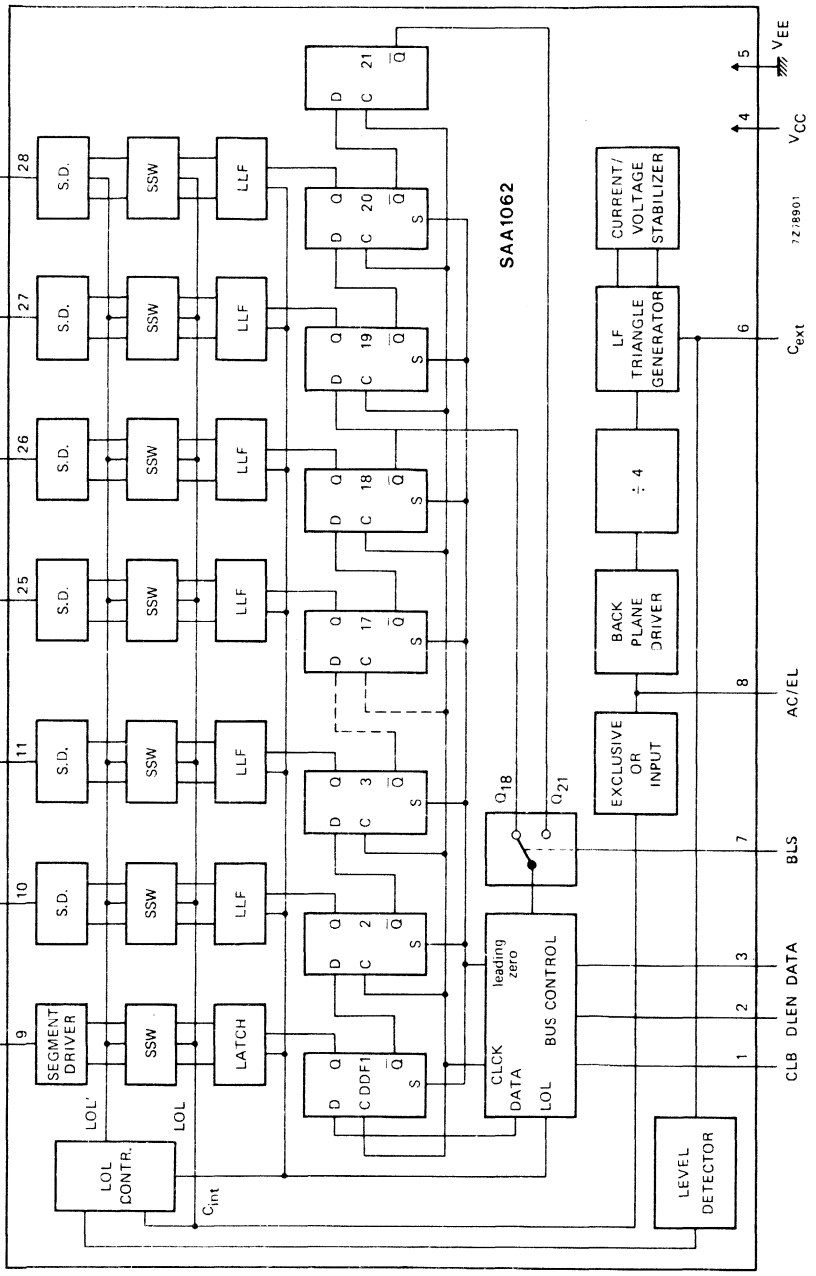


Fig. 2 Block diagram.

OPERATION DESCRIPTION

The input information for this device consists of a data bus with 18 or 21 bits words, an external clock synchronized with the data bus and an enable signal. The organization of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is made whether these signals are valid for the device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal is HIGH, during the first HIGH period of the clock signal. During the HIGH period of DLEN, the length control determines if the clock signal consists of the programmed number of pulses (18 or 21). This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device from accepting inferferences on the signal lines. While leading zero is detected, the shift register is set and for a proper leading zero the following data is shifted into this register. The Q_n position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input are correct. Incorrect length of the information is detected by checking the value of the last bit of the programmed register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOL). This pulse enables the load control circuit to load the contents of the register into the latch. On the first edge of the backplane driver signal 'AC out EL in' following on this 'LOL' pulse, the new information of this latch is transferred to the output driver which also contains a latch. In the static mode this transfer is done immediately on the LOL pulse. With this ability it is possible to load the device with 20 bits and to transfer this data to the segment outputs; the SR and latches will be reloaded by a second complete load procedure without an 'AC out' edge, and then another reload without a load enable clock pulse which makes the SR contents 20 bits, the latches 20 bits and the output latches 20 bits of information.

The l.f. oscillator consists of a triangle generator of the I-2I principle. It only needs an external capacitor to fix the frequency. As both amplitude and current are temperature compensated, this frequency is more or less independent of pn temperature. An internal switching signal of this generator is divided by 4 to attain a symmetrical output for the backplane driver (pin 8) of nominal 60 Hz for an external capacitor of 22 nF.

The backplane driver is able to drive a 40 bits display. When C_{ext} (pin 6) is connected to ground or V_{CC}, the device acts as a synchronized or static slave. In this case the backplane driver is switched-off and pin 8 only acts as the 'EL in' input.

The bit length of the shift register is programmed with BLS (Bit Length Selector) (pin 7). If BLS is kept LOW the DATA bit length is 20; for BLS open or HIGH a DATA bit length of 17 is selected.

DEVELOPMENT SAMPLE DATA

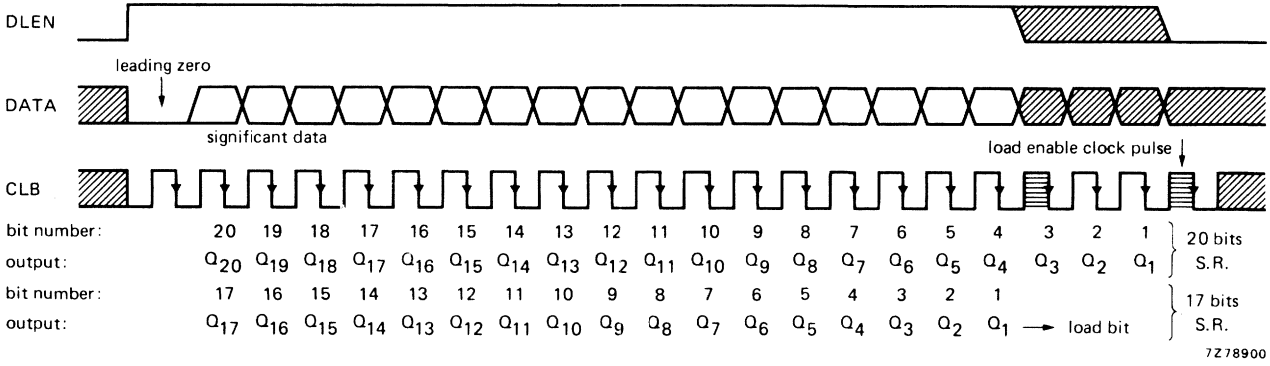


Fig. 3 Organization of 18 and 21 bits words; DATA = LOW means segment 'on'.

GENERAL DESCRIPTION

A frequency indicator system can be made with the SAA1070 and the frequency divider SAA1058. It has the following features:

- A 4½-digit LED display driver. Action starts in duplex mode: the indicators are driven by half sine-wave pulses, the two character groups are switched during the zero crossing of the duplex phases. This will obtain minimum interference at correct exploitation of the terminals.
- An 18-bit frequency counter with display decoder and indicator memory. The counter can be preset in a wide range of programmed offset frequencies, so it is possible to obtain, independent of each other, 15/24 different i.f. signals in the FM, SW, MW and LW ranges.
- A timing unit driven by a 4 MHz quartz crystal on the chip.
- A 16-bit comparator for loading the measured frequencies. The frequency value in the display latch will only be changed when three successive counter values are different to the latch values. This eliminates display flicker for interferences and reduces the sensibility.
- Latch loading; in this case the frequency counter and the prescaler are stopped and the last measured frequency is displayed continuously.
- In FM operation choice of displaying received frequency or channel number.
- Display test and blanking facilities.

OPERATION DESCRIPTION

The timing for a measurement cycle is started at a positive-to-negative transition of input DUP (pin 16). The internal timing unit generates pulses of different length in which the programmed i.f. signals will be determined (see Tables 1 and 2). During this time the driver outputs Q_1 to Q_9 are internally switched as inputs; the driver outputs are blocked. The programming of a '1' or '0' is achieved by using or omitting 22 kΩ resistors between the appropriate output and pin 15 (Q_{1F}), or between these outputs and + 2,5 V (see Fig. 4).

The counter is preset (parallel i.f. presetting) depending on the i.f. chosen and the mode of operation (FM, SW, MW and LW, see Table 3). This is followed by serial offset; the counter then has a pulse train applied via a gating circuit, the number of pulses also depends on the programming of Q_1 to Q_9 and the mode of operation. The gating circuit releases input FIN (pin 12) for a defined time, in which the applied pulse to FIN switches the counter.

A HIGH level is obtained at output GATE (pin 13) during this specified measuring time; after that the 16 most significant bits of the counter will be compared with the contents of the latch. If an unequal content is detected a 2-bit comparator counter is incremented: an equal state of the comparator resets this counter. As soon as the comparator counter is in position 3, i.e. after three successive different counter values, the new counter contents will be transferred to the latch at the following positive-to-negative transition of signal DUP. The latch value will be decoded for a 7-segment display and transferred to the LED outputs Q_1 to Q_{15} via a duplex circuit. The LED segments have to be connected to the display outputs via current-limiting resistors (as explained above).

Table 1. Setting of i.f. offset frequencies for FM operation.
Wavelength control: WLC = F.C.

pin number				offset frequency
27	24	23	20	MHz
0	0	0	0	10,7000
0	0	0	1	10,6000
0	0	1	0	10,6125
0	0	1	1	10,6250
0	1	0	0	10,6375
0	1	0	1	10,6500
0	1	1	0	10,6625
0	1	1	1	10,6750
1	0	0	0	10,6875
1	0	0	1	10,7000
1	0	1	0	10,7125
1	0	1	1	10,7250
1	1	0	0	10,7375
1	1	0	1	10,7500
1	1	1	0	10,7625
1	1	1	1	10,7750

0 = no resistor.
1 = 22 kΩ resistor to + 2,5 V (see Fig. 4).

Table 2. Setting of i.f. offset frequencies for AM operation.
Wavelength control: WLC = S.ML.

pin number					offset frequency kHz	
28	26	25	22	21	S	ML
0	0	0	0	0	460,00	460
0	1	0	0	0	448,75	449
0	1	0	0	1	450,00	450
0	1	0	1	0	451,25	451
0	1	0	1	1	452,50	452
0	1	1	0	0	453,75	453
0	1	1	0	1	455,00	454
0	1	1	1	0	456,25	455
0	1	1	1	1	457,50	456
1	0	0	0	0	456,25	457
1	0	0	0	1	457,50	458
1	0	0	1	0	458,75	459
1	0	0	1	1	460,00	460
1	0	1	0	0	461,25	461
1	0	1	0	1	462,50	462
1	0	1	1	0	463,75	463
1	0	1	1	1	465,00	464
1	1	0	0	0	463,75	465
1	1	0	0	1	465,00	466
1	1	0	1	0	466,25	467
1	1	0	1	1	467,50	468
1	1	1	0	0	468,75	469
1	1	1	0	1	470,00	470
1	1	1	1	0	471,25	471
1	1	1	1	1	472,50	472

OPERATION DESCRIPTION (continued)

The operation mode of the circuit depends on the state of the wavelength control inputs (pins 8 to 11); see Table 3.

Table 3. Truth table of the WLC inputs.

operation mode	wavelength control inputs F (pin 10)	C (pin 11)	S (pin 9)	ML (pin 8)
v.h.f. frequency (FM)	0	1	1	1
v.h.f. channel (FM)	X	0	1	1
short wave	1	X	0	1
medium wave	1	X	1	0
long wave	1	X	1	0
display test	0	0	1	0
display blanking	0	X	0	X
display blanking	1	X	0	0
display blanking	0	1	1	0
display blanking	1	1	1	1

0 = 0 V (ground)
1 = +5 V
X = state is immaterial

The display position and resolution of the frequency measurement is given in Table 4.

Table 4.

operation mode	display range (number of indicators) min. 1	2	3	4	5	max. 1	2	3	4	5		resolution
v.h.f. frequency (FM)		0	0	0	0	1	9	9	9	5*	MHz	0,05 MHz
v.h.f. channel (FM) ▲	–		0	0		+		9	9	**		0,1 MHz
short wave		0	0	0	0	1	9	9	9	5	kHz	5,0 kHz
medium/long wave		0	0	0		1	9	9	9		kHz	1,0 kHz

* Limited to 109,30 MHz for a maximum input frequency of 3,75 MHz.
** Limited to −64 for a maximum input frequency of 3,75 MHz.
▲ One channel = 300 kHz; e.g. channel 02 = 87,6 MHz

The display frequency corresponds to the frequency to be measured, at an input frequency f_{in} at pin 12:

$$f_{in} = \frac{f_m + f_{offset}}{32}$$

in which: f_{in} = input frequency,
f_m = frequency to be measured,
f_{offset} = i.f. offset frequency programmed as is Tables 1 and 2.

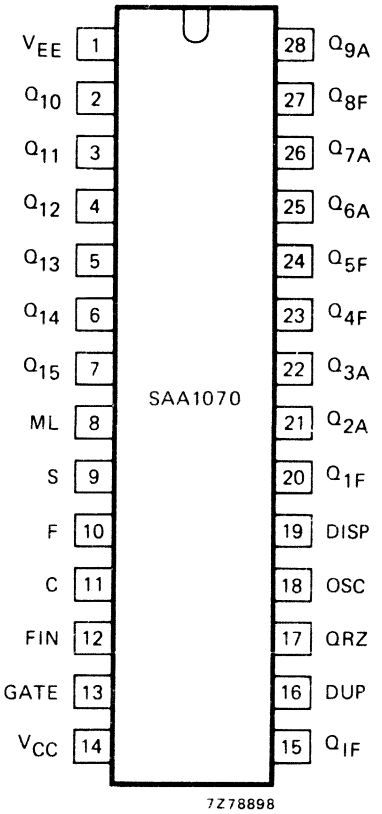


Fig. 2 Pinning diagram.

PINNING

14	V_{CC}	positive supply
1	V_{EE}	negative supply (0 V, ground)

Inputs

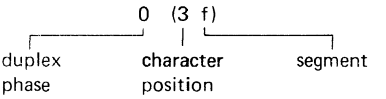
8	ML	medium and long wave
9	S	short wave
10	F	FM
		} wavelength control; when connected to ground
11	C	channel control when connected to ground; other functions can be obtained by connecting more wavelength control inputs to ground simultaneously (see Table 3).
12	FIN	input for frequency to be measured
16	DUP	synchronization of the internal timing unit and selection of the character groups (duplex input)
17	QRZ	input for the quartz-crystal oscillator

PINNING (continued)

19	DISP	control input for mode of operation open: comparator operates grounded: stop display is obtained; the timing unit is stopped in position 20 and cannot be started again by the duplex input (DUP); the last displayed value remains stored in the latches and is driven to the output; the comparator counter is reset; output GATE (pin 13) is LOW at V_{CC}: the comparator function is switched-off; the contents of the counter are loaded into the latches every period 18 of the timing unit; the timing unit will also be stopped at the beginning of period 17 independent of the state of the comparator output; in that case the display rate will be higher

Inputs/outputs

The following notation is used for the LED driver outputs:



e.g. 1 (4a) means: on duplex input = 1; the 'a' segment of the fourth digit is driven.

20	Q_{1F}	LED output 0 (3f); 1 (2f) i.f. offset input 1 for FM
21	Q_{2A}	LED output 0 (3g); 1 (2g) i.f. offset input 1 for AM
22	Q_{3A}	LED output 0 (3e); 1 (2e) i.f. offset input 2 for AM
23	Q_{4F}	LED output 0 (3d); 1 (2d) i.f. offset input 2 for FM
24	Q_{5F}	LED output 0 (3c); 1 (2c) i.f. offset input 3 for FM
25	Q_{6A}	LED output 0 (3b); 1 (2b) i.f. offset input 3 for AM
26	Q_{7A}	LED output 0 (3a); 1 (2a) i.f. offset input 4 for AM
27	Q_{8F}	LED output 0 (5g); 1 (4b) i.f. offset input 4 for FM
28	Q_{9A}	LED output 0 (1d); 1 (4f) i.f. offset input 5 for AM

Outputs

2	Q_{10}	LED output 0 (5a, 5d); 1 (4a)
3	Q_{11}	LED output 0 (5b, 5e); 1 (4c)
4	Q_{12}	LED output 0 (5c, 5f); 1 (4d)
5	Q_{13}	LED output 0 (1c); 1 (4g)
6	Q_{14}	LED output 0 (1a, 1b); 1 (4e)
7	Q_{15}	LED output 0 (3h, MHz indicator); 1 (kHz indicator)
15	Q_{IF}	i.f. offset control output; this output is set to 2,5 V at the beginning of a measuring period; when programming resistors are connected to this pin, it must also be connected to both phases of the LED anode voltages via diodes; this prevents a segment being switched off by the programming resistors.
13	GATE	open collector output; counter is active when this pin is HIGH; also used to drive the reset input of the divide by 32 prescaler (SAA1058)
18	OSC	output for the quartz-crystal oscillator

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}	−0,5 to + 7	V
Total power dissipation	P_{tot}	max. 900	mW
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Storage temperature range	T_{stg}	−25 to + 125	°C

CHARACTERISTICS

V_{EE} = 0; V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.	
Supply voltage	V_{CC}	4,5	5	5,5	V
Supply current	I_{CC}	–	90	–	mA
Inputs ML, S, F, C					
open voltage	V_{IO}	2,5	4,5	–	V
input voltage HIGH	V_{IH}	2,0	–	5,0	V
input voltage LOW	V_{IL}	0	–	1,0	V
input current LOW; V_{IL} = 1 V	$-I_{IL}$	30	–	300	μA
Input DUP					
input voltage HIGH	V_{IH}	1,0	–	12,0	V
input voltage LOW	V_{IL}	−6,0	–	0,4	V
input resistance HIGH	R_{IH}	0,6	–	1,5	kΩ
Input FIN					
input voltage HIGH	V_{IH}	2	–	5	V
input voltage LOW	V_{IL}	0	–	1	V
input current HIGH	I_{IH}	–	–	20	μA
input capacitance	C_I	–	–	4	pF
input frequency	f_I	–	–	3,75	MHz
Inputs Q_{1F}, Q_{2A}, Q_{3A}, Q_{4F}, Q_{5F}, Q_{6A}, Q_{7A}, Q_{8F}, Q_{9A}					
input voltage HIGH	V_{IH}	1,8	–	12	V
open voltage (logic LOW)	V_{IO}	0,2	1,4	1,5	V
input current HIGH	I_{IH}	10	20	30	μA
programming resistor between input and pin 15 (at 2,5 V for HIGH)	R_{IF}	15	22	33	kΩ
I.F. offset					
accuracy; WLC = F.C.		–	–	± 8	kHz
accuracy; WLC = S.M.L.		–	–	± 0,6	kHz
supply sensitivity; WLC = F.C.		–	–	10	kHz/V
supply sensitivity; WLC = S.M.L.		–	–	0,8	kHz/V

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	
Input DISP					
open voltage HIGH (note 1)	V_{OH}	0,6	–	0,8	V
open voltage LOW (note 1)	V_{OL}	0	–	0,4	V
input voltage LOW	V_{IL}	−0,4	0	0,4	V
input voltage HIGH	V_{IH}	2,0	–	5,0	V
Outputs Q_{1A}, Q_{2A}, Q_{3A}, Q_{4F}, Q_{5F}, Q_{6A}, Q_{7A}, Q_{8F}, Q_{9A}, Q_{13}					
output voltage HIGH	V_{QH}	–	–	12	V
output voltage LOW; I_{QL} = 40 mA	V_{QL}	–	–	0,5	V
output current LOW; note 2	I_{QL}	–	–	60	mA
Outputs Q_{10}, Q_{11}, Q_{12}, Q_{14}, Q_{15}					
output voltage HIGH	V_{QH}	–	–	12	V
output voltage LOW; I_{QL} = 80 mA	V_{QL}	–	–	0,5	V
output current LOW; note 2	I_{QL}	–	–	120	mA
Oscillator connections OSC, QRZ					
frequency	f	–	4,0	–	MHz
input voltage HIGH; QRZ	V_{IH}	2,6	–	5,0	V
input voltage LOW; QRZ	V_{IL}	−2,0	–	2,0	V
input resistance QRZ	R_I	50	–	–	kΩ
input capacitance QRZ	C_I	–	–	5,0	pF
open voltage QRZ	V_{IO}	–	2,25	–	V
open voltage OSC	V_{IO}	–	1,5	–	V
Output GATE					
output voltage LOW; I_{QL} = 20 mA	V_{QL}	–	–	1,0	V
output voltage HIGH; I_{QH} = 0	V_{QH}	–	–	12	V
Output Q_{IF}					
output voltage; conductive	V_Q	2,2	2,5	2,8	V
output voltage; non-conductive	V_Q	–	–	12	V
output resistance; conductive	R_Q	350	500	650	Ω
output resistance; non-conductive	R_Q	50	–	–	kΩ

Notes

1. When this pin is left open it acts as an output at which the number of serial offset pulses for the i.f. offset can be obtained.
2. Peak current for sinusoidal voltage.

APPLICATION INFORMATION

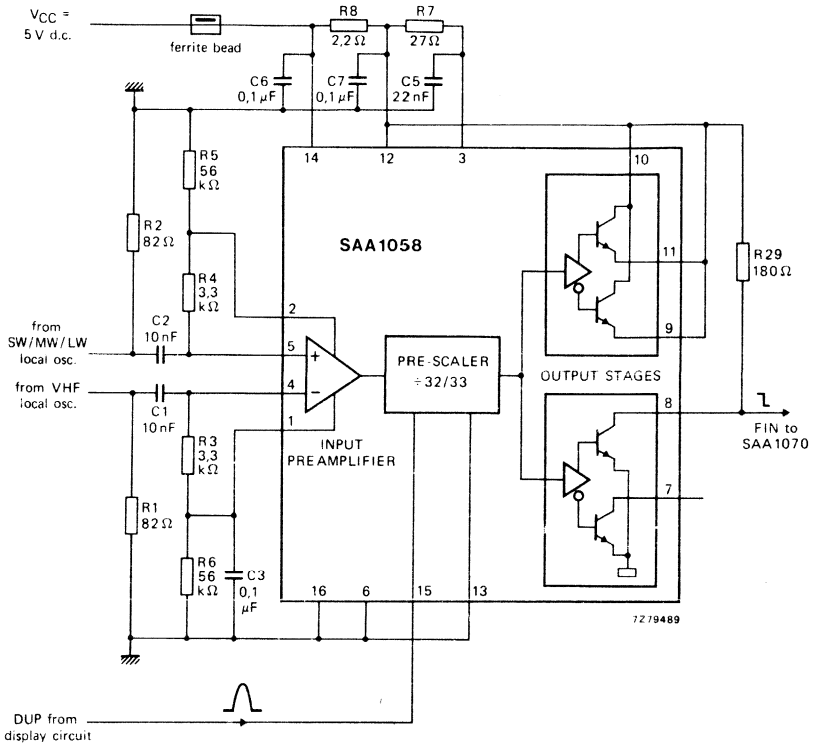


Fig. 3 Pre-scaler circuit for the frequency measurement system; to be used in combination with Fig. 4.

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION (continued)

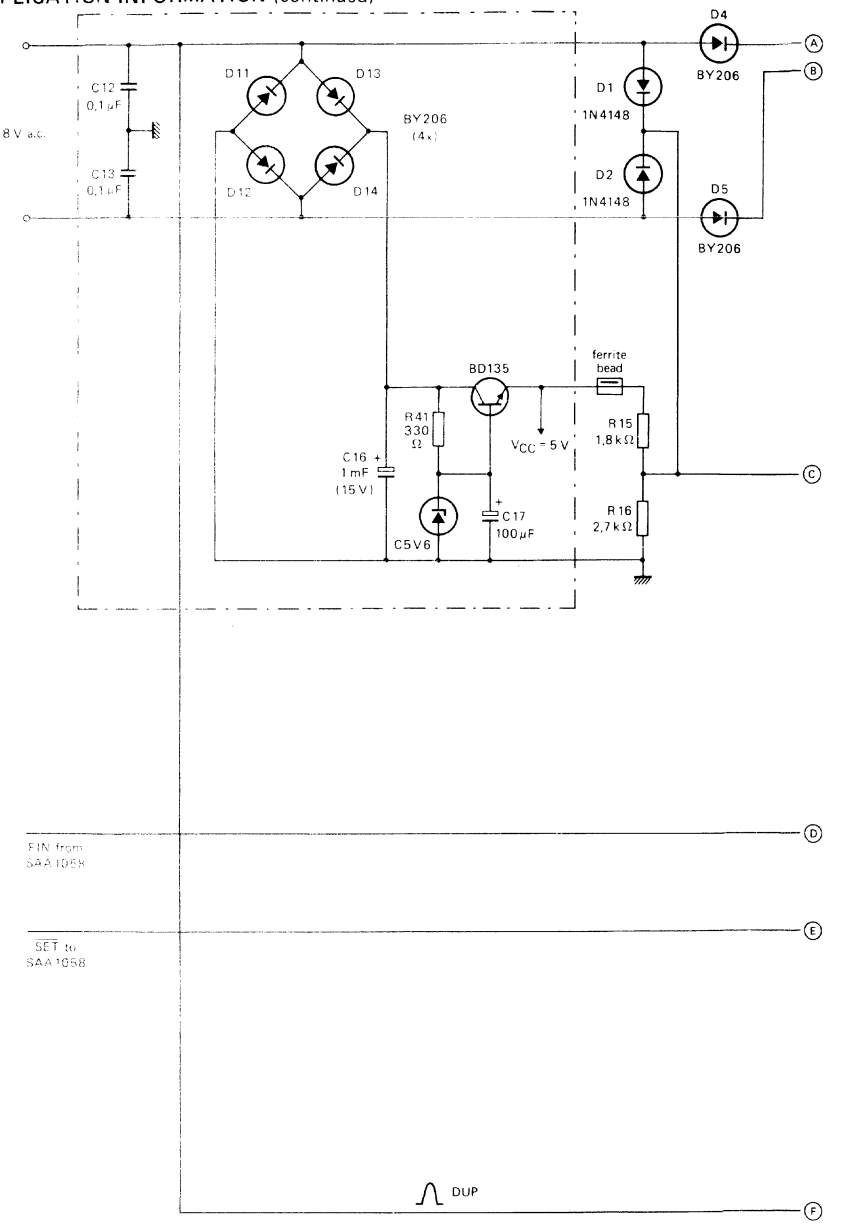
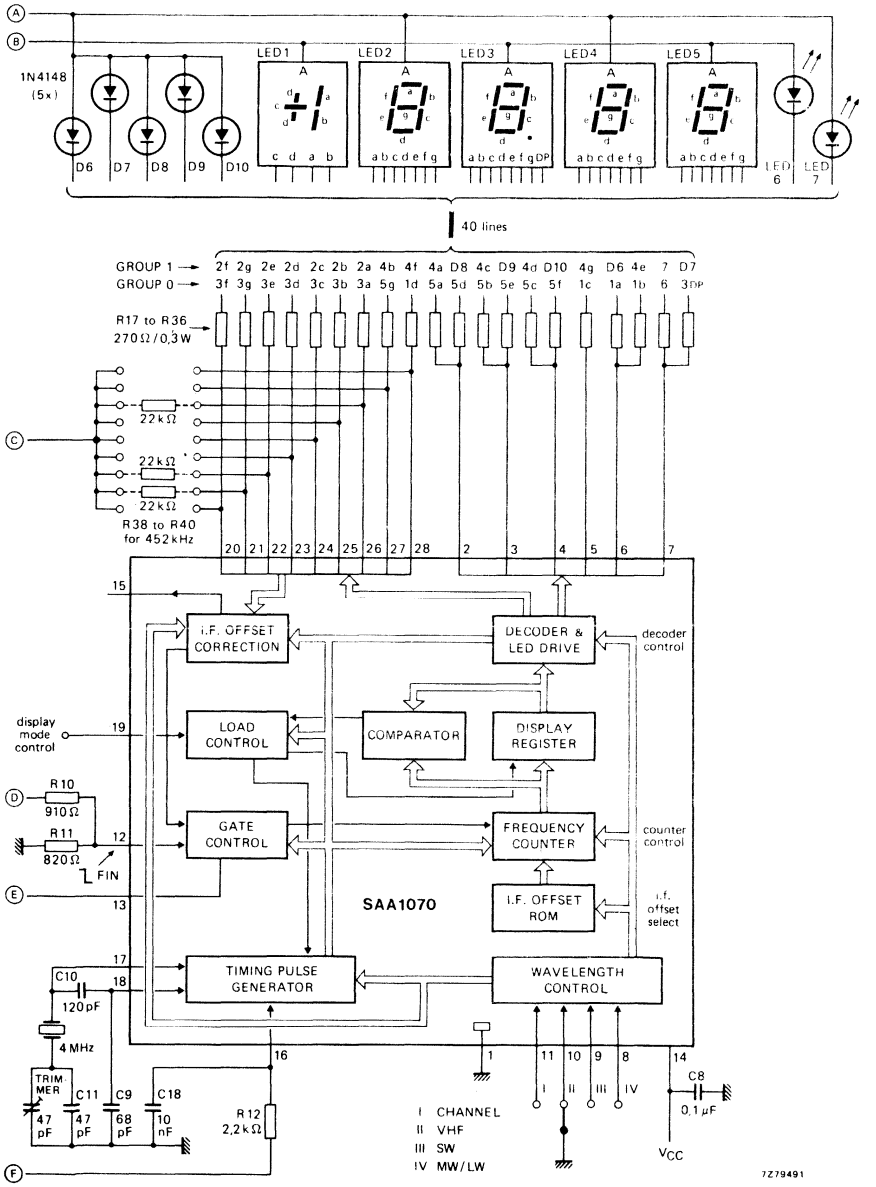


Fig. 4 Display drive circuit for the frequency measurement system; continued on next page (see also Fig. 3).


1N4148
(5×)
D6
D7
D8
D9
D10
LED1
LED2
LED3
LED4
LED5
LED 6
LED 7
40 lines
GROUP 1
GROUP 0
R17 to R36
270Ω/0,3W
22kΩ
22kΩ
22kΩ
R38 to R40
for 452kHz
i.f. OFFSET CORRECTION
DECODER & LED DRIVE
decoder control
display mode control
LOAD CONTROL
COMPARATOR
DISPLAY REGISTER
R10
910Ω
R11
820Ω
FIN
GATE CONTROL
FREQUENCY COUNTER
counter control
SAA1070
I.F. OFFSET ROM
i.f. offset select
TIMING PULSE GENERATOR
WAVELENGTH CONTROL
C10
120pF
4MHz
TRIM-MER
47 pF
C11
47 pF
C9
68 pF
C18
10 nF
R12
2,2kΩ
I CHANNEL
II VHF
III SW
IV MW/LW
C8
0,1μF
VCC
7Z79491

REMOTE CONTROL TRANSMITTER ENCODER

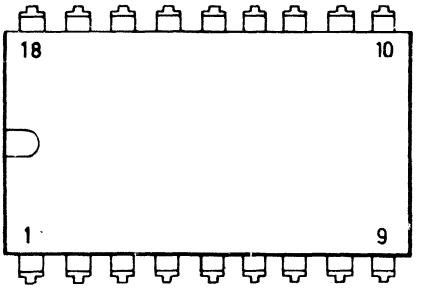
The SAA5000 is a MOS N-channel integrated circuit which provides the encoding and modulation functions for the remote control of television receivers, including those equipped with teletext and viewdata facilities.
It is intended for use with the SAA5010 remote control receiver decoder device. 32 commands are provided which can be activated by either touch or switch controls.
Modulation may be selected for either infra-red or ultrasonic transmission systems.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	6	V
Supply current (Inactive, $I_{DD} + I_{16}$)		<	20	μA
(Active, I_{DD})		typ.	25	mA
Number of commands			32	
Power-up			Automatic	
Operating temperature range	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A)



Viewed from top

PINNING

1. V_{SS}
2. Oscillator (C and R common connection)
3. Oscillator (R connection)
4. } Keyboard (Matrix inputs)
5. }
6. }
7. }
8. }
9. }
10. } Keyboard (Matrix outputs)
11. }
12. }
13. }
14. }
15. }
16. $\overline{\text{Data}}$ output (Modulator drive)
17. Ultrasonic/Infra-red select
18. V_{DD}

DESCRIPTION

The method of data encoding provides a 24-bit code which incorporates protection against false responses at the decoder under adverse transmission path conditions.
The device automatically "powers up" when the first command is selected and reverts to the standby mode when the operation has been completed. No adjustments or critical components are required in the peripheral circuitry.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See MOS Handling Notes).

RATINGS Limiting values in accordance with the Absolute Maximum System.

		min.	max.	
Voltages				
Supply voltage (pin 18)	V_{DD}	−0.3	7.5	V
$\overline{\text{Data}}$ output (Modulator drive) (pin 16)		−0.3	11.0	V
Input voltage – all inputs (pins 2 to 9 and 17)		−0.3	7.5	V
Output voltage – all outputs except pin 16 (pins 10 to 15)		−0.3	7.5	V
Temperatures				
Storage temperature	T_{stg}	−20 to +125		°C
Operating ambient temperature	T_{amb}	−20 to +70		°C
$\overline{\text{Data}}$ output				
Safe duration for short circuit to V_{DD}			1	s

CHARACTERISTICS

		min.	typ.	max.	
Supply voltage (pin 18)	V_{DD}	4.5	–	7.0	V

The following characteristics apply at T_{amb} = 25 °C, V_{DD} = 6 V unless otherwise stated.

Supply current					
Inactive, $I_{DD} + I_{16}$		–	–	20	μA
Active, I_{DD}		–	25	35	mA
Oscillator (pins 2 and 3)					
Operating bit period (V_{DD} = 4.5 to 7 V, C = 1.0 nF, R = 220 kΩ)		6.5	8.2	10	ms
Keyboard Matrix inputs (pins 4 to 9)					
Switching threshold voltage		0.95	–	1.45	V
Keyboard Matrix outputs (pins 10 to 15)					
Output voltage HIGH state					
V_{DD} = 4.5 V	I_{out} = −10 μA	4.3	–	–	V
V_{DD} = 4.5 V	I_{out} = −125 μA	2.25	–	–	V

	min.	typ.	max.	
Output voltage. LOW state				
V_{DD} = 7.5 V	–	–	0.48	V
Short circuit current	–	–	0.95	mA
$\overline{\text{Data}}$ output (Modulator drive) (pin 16)				
Low-state voltage (I_{16} = 15 mA)	–	–	0.5	V
Pull-down transition time	–	–	2	μs
Infra-red operation				
Low-state duration				
(Expressed as a ratio of bit period)	–	1:24	–	
Ultrasonic operation				
'0' bit low state duration				
(Expressed as a ratio of bit period)	–	1:6	–	
'1' bit low state duration				
(Expressed as a ratio of bit period)	–	4:6	–	

APPLICATION DATA

Data bit period and response time

The data bit period is controlled by choice of the two oscillator timing components connected to pins 2 and 3. Table 1 shows oscillator timing component values against data bit period.

Ultrasonic operation (Fig.2)

The system response time is approximately 27 x bit period. The minimum bit period is limited by ultrasonic echo decay time encountered under operational conditions and for reliable operation a nominal bit period of 8.2 ms is recommended. Transmitter supply current for the recommended circuit shown in Fig. 2 is approximately 3 mA r.m.s., and is independent of the data bit period.

Infra-red operation (Fig.3)

The system response time is approximately 51.5 x bit period. The transmitter stage (recommended circuit shown in Fig. 3) supply current varies with the bit period as shown in Table 1.

Table 1

Oscillator resistor = 220 kΩ

Oscillator capacitor (pF)		100	120	150	180	220	270	330	390	470	560	680	820	1000	1200
Bit period	(ms)	0.82	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2	10
Transmitter stage average current	Infra-red (mA)	23	19	16	13	11	8.7	7.0	5.8	4.9	4.1	3.4	2.8	2.3	1.9
	Ultrasonic (mA)	3	3	3	3	3	3	3	3	3	3	3	3	3	3

APPLICATION DATA (continued)

The function is quoted against the corresponding pin number

Pin No.

1. V_{SS} Ground – 0 V

2, 3 **Oscillator timing components**

A resistor and capacitor are required to time the oscillator, the frequency of which determines the output data bit rate. The capacitor is connected between pins 1 and 2 and the resistor between pins 2 and 3.

4, 5, 6, 7, 8, 9 **Keyboard Inputs** (From keyboard matrix)

10, 11, 12, 13, 14, 15 **Keyboard Outputs** (To keyboard matrix)

In the 'powered down' state these outputs assume approximately the battery +ve potential. The required data code sequence (see Table 2) is selected by connecting a chosen input to one of the outputs via the keyboard matrix. The application of the high level from the output to the input causes the circuit to 'power-up', the oscillator starts and a sequence of pulses appear on the output pins. As a result of the connection between the selected input and output the chosen message code appears at the data output (pin 16). When the connection is removed the circuit returns to the 'powered-down' state at the end of the message sequence.
Input sensitivity is controlled by the choice of the input pull-down resistors. For maximum sensitivity (i.e. for touch sensitive keyboards) 6.8 MΩ resistors are recommended. Lower values can be used (18 kΩ minimum) with low impedance keyboard switches.

16. **$\overline{\text{Data}}$ output** (Modulator drive)

This is an open-drain output capable of sinking current to V_{SS}. In the 'powered down' state the output is high impedance. When the circuit is active the 24 bit data sequence appears at this output to control an ultrasonic or infra-red transmitter. (See Fig. 5 for details of the data pulse train). When infra-red mode is selected the 24 bit sequence is transmitted twice with an extra pulse at the end of each sequence. This is to ensure the correct reception of the code by the receiver.

17. **Ultrasonic/Infra-red s**elect

By connecting this pin to V_{SS} the data output pulses are suitable for ultrasonic transmission. By connecting this pin to V_{DD} the output pulses are suitable for infra-red transmission. (See Fig. 4 for details of data pulses).

18. V_{DD} Positive Supply

A 6 V dry cell battery may be used for operation in a portable unit. Four HP7 cells, or equivalent, are recommended.

Peripheral circuitry

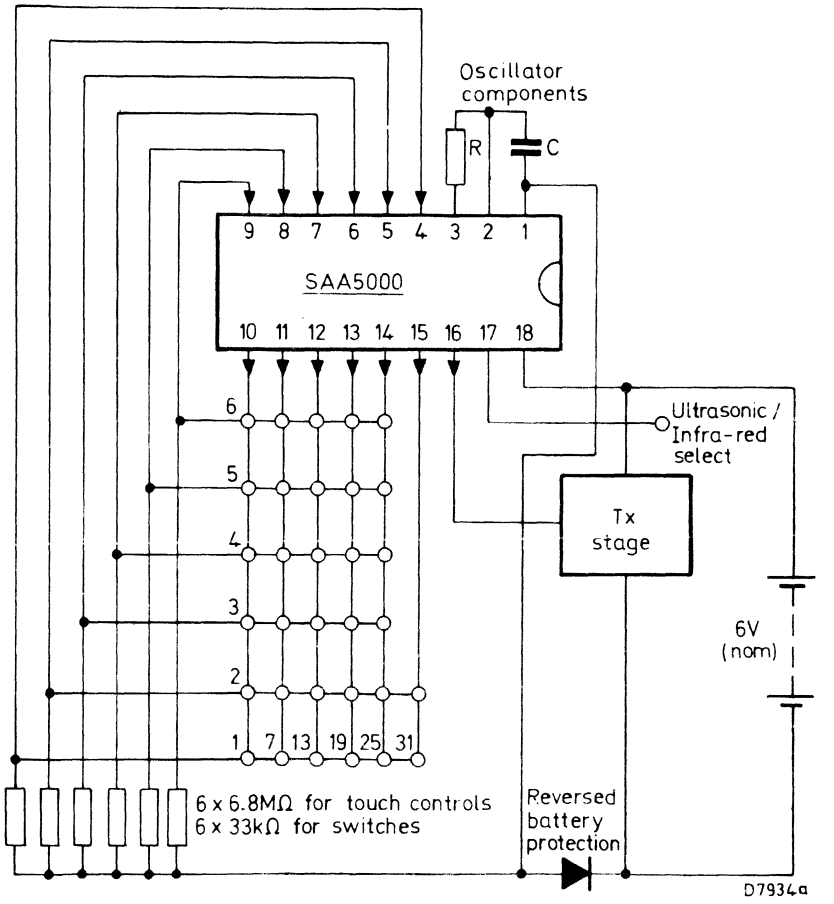


Fig.1

APPLICATION CIRCUITS

Ultrasonic Transmitter

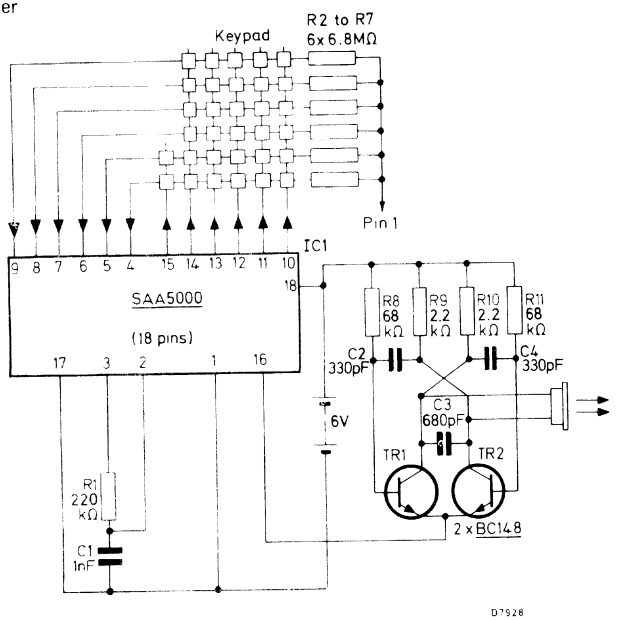


Fig.2

Infra-red Transmitter

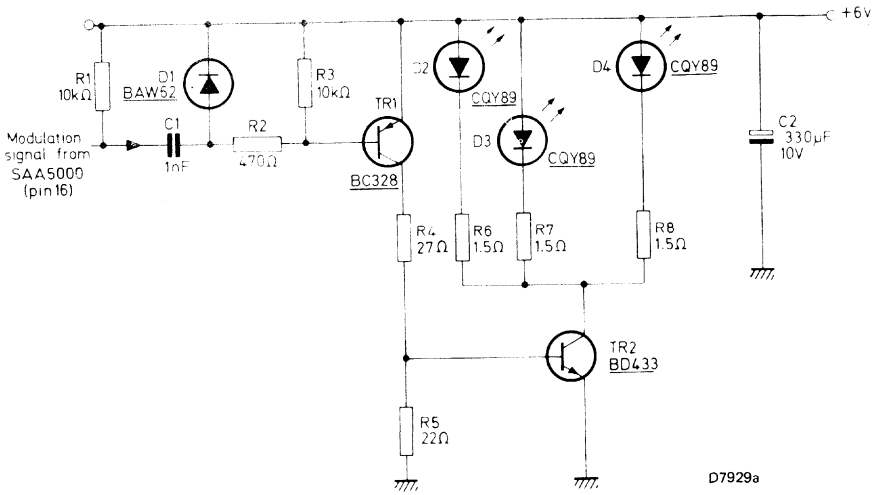


Fig.3

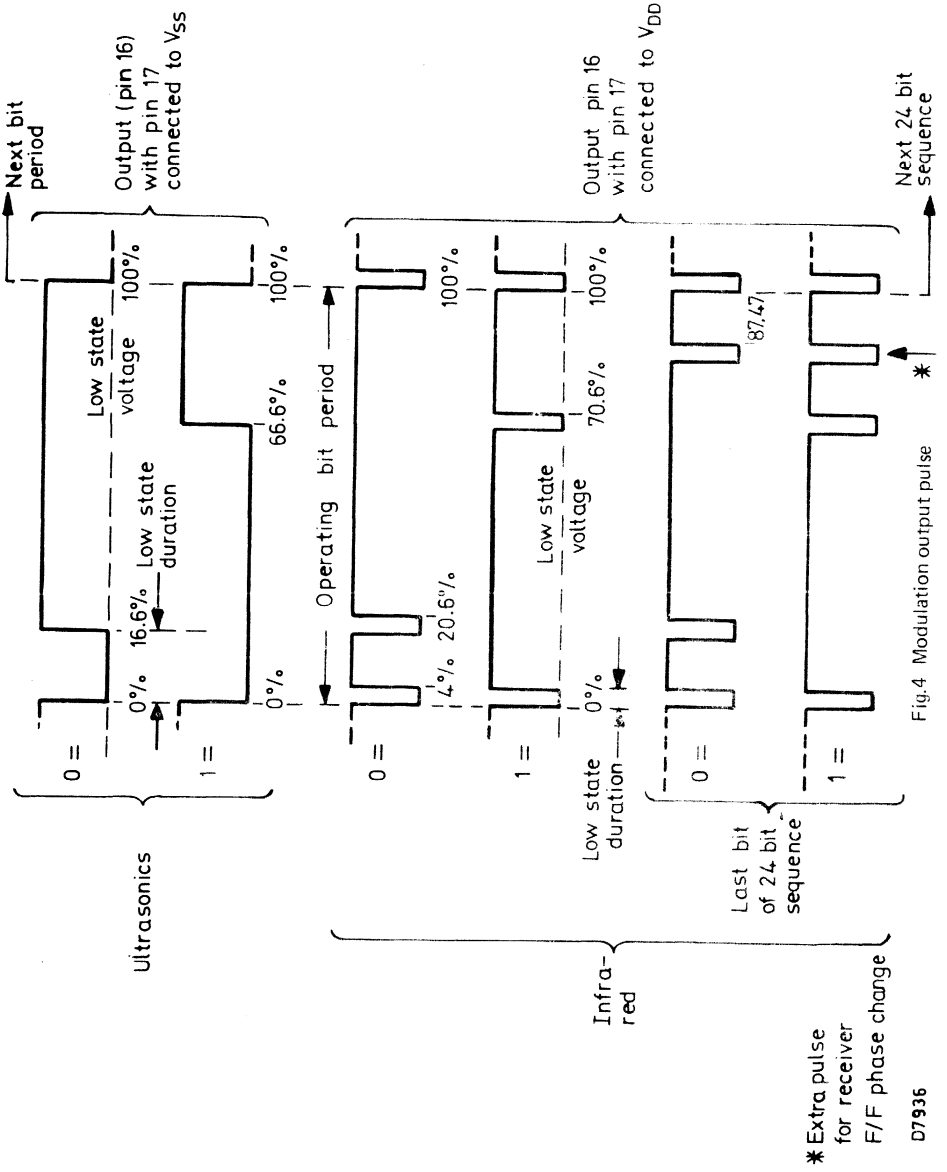


Fig.4 Modulation output pulse

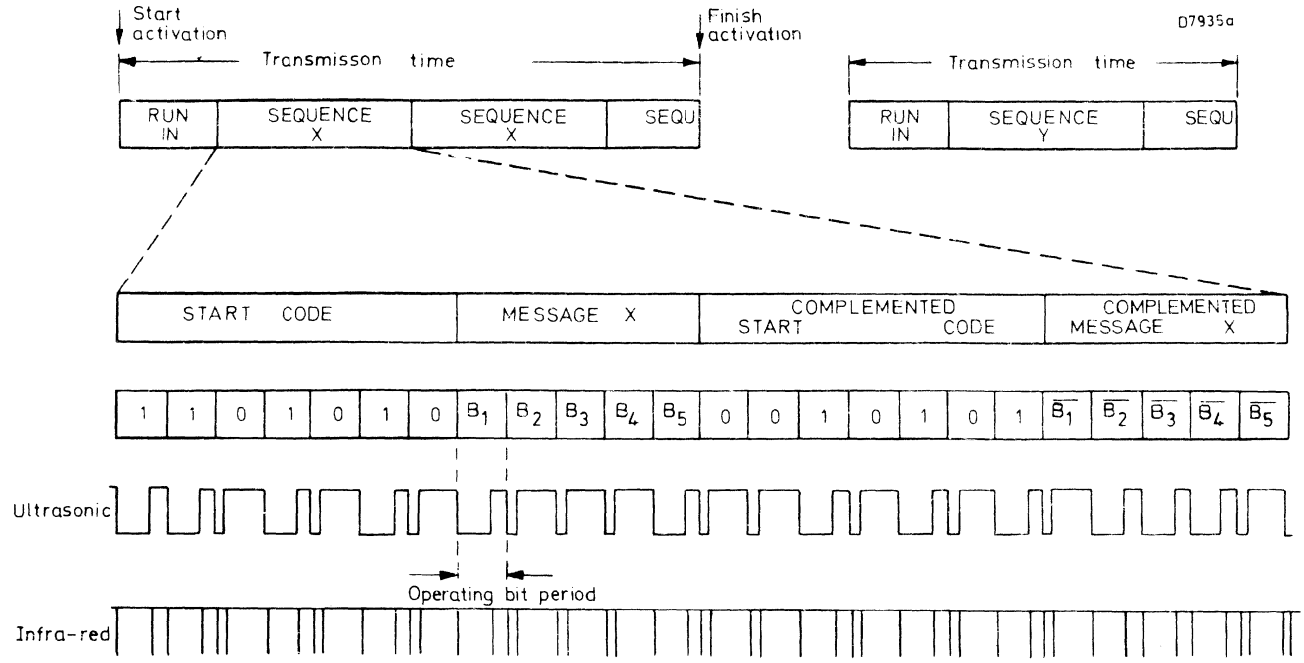


Fig.5 Encoded data format (example: code 18)

See Fig. 4 for details of output pulses.

Transmitter message code

Table 2

Key No.	Binary code				
	B_1	B_2	B_3	B_4	B_5
1	0	0	0	0	0
2	1	0	0	0	0
3	0	1	0	0	0
4	1	1	0	0	0
5	0	0	1	0	0
6	1	0	1	0	0
7	0	1	1	0	0
8	1	1	1	0	0
9	0	0	0	1	0
10	1	0	0	1	0
11	0	1	0	1	0
12	1	1	0	1	0
131	0	0	1	1	0
14	1	0	1	1	0
15	0	1	1	1	0
16	1	1	1	1	0

Key No.	Binary code				
	B_1	B_2	B_3	B_4	B_5
17	0	0	0	0	1
18	1	0	0	0	1
19	0	1	0	0	1
20	1	1	0	0	1
21	0	0	1	0	1
22	1	0	1	0	1
23	0	1	1	0	1
24	1	1	1	0	1
25	0	0	0	1	1
26	1	0	0	1	1
27	0	1	0	1	1
28	1	1	0	1	1
29	0	0	1	1	1
30	1	0	1	1	1
31	0	1	1	1	1
32	1	1	1	1	1

REMOTE CONTROL RECEIVER DECODER

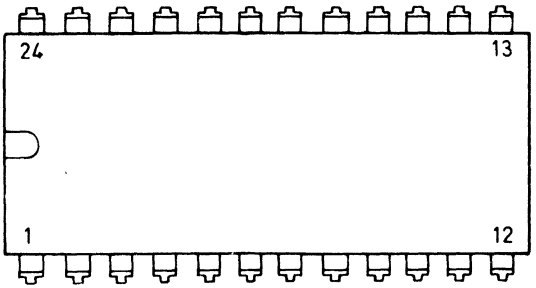
The SAA5010 is a MOS N-channel integrated circuit which provides the receiver decoding function for the remote control of television receivers.
The SAA5010 is a 24-lead device for the control of television receivers incorporating stepable tuning selector systems and including those equipped with teletext and viewdata facilities. It is suitable for use either in ultrasonic or infra-red transmission systems and is intended for use with the SAA5000 transmitter encoder integrated circuit. The SAA5010 is also suitable for direct connection to the SAA5040 and the SAA5050 teletext decoder circuits. Operation with the digital channel selection system (DICS) is also possible.

QUICK REFERENCE DATA

Supply voltage				
Digital	V_{DD1}	nom.	5	V
Analogue	V_{DD2}	nom.	12	V
Supply current				
Digital	I_{DD1}	typ.	20	mA
Analogue	I_{DD2}	typ.	10	mA
Operating temperature range	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)



Viewed from top

PINNING

1 - V_{SS}
2 - Local reset
3 - Step
4 - Clear
5 - $\overline{\text{Data}}$ out
6 - On/standby
7 - DLIM
8 - $\overline{\text{DLEN}}$
9 - Mute
10 - Analogue 1
11 - Analogue 2
12 - Analogue rate of change control
13 - V_{DD2}
14 - Analogue 3
15 - Analogue 4
16 - Message received indicator
17 - Picture on sense
18 - Oscillator (R connection)
19 - Oscillator (C and R common connection)
20 - Teledata modes inhibit
21 - Clock out
22 - Data input
23 - Data input type selector
24 - V_{DD1}

DESCRIPTION

The data input is in the form of a 7-bit framing code and a 5-bit message followed by an identical but complemented sequence making a complete 24-bit message sequence. Error checking is effected within the device to ensure a high degree of corrupted signal immunity. The SAA5010 allows for 16 channel selections, 4 analogue functions (e.g. volume, contrast, brightness and saturation), sound muting, and 'set in standby' to be controlled remotely. An output is provided to drive visual and/or audible indication of a received code. Logic outputs are available to provide control data and clocks for use in teletext, viewdata and DICS systems. No adjustments or critical components are required in the peripheral circuitry.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See MOS Handling Notes).

RATINGS

Limiting values of operation in accordance with the Absolute Maximum System.

		min.	max.	
Voltages (with respect to pin 1)				
Supply voltage (pin 24)	V_{DD1}	−0.3	7.5	V
(pin 13)	V_{DD2}	−0.3	14	V
Input voltages All inputs except Data in and Picture on sense (pins 2, 12, 18, 19, 20, 23)		−0.3	7.5	V
Data in and Picture on sense (pins 22, 17)		−0.3	14	V
Output voltage All outputs to TV functions (pins 3, 4, 6, 9, 10, 11, 14, 15, 16)		−0.3	14	V
Logic outputs (pins 5, 7, 8, 21)		−0.3	7.5	V

Temperatures

Storage temperature	T_{stg}	−20 to +125	°C
Operating ambient temperature	T_{amb}	−20 to +70	°C

CHARACTERISTICS

Supply voltages	min.	typ.	max.	
V_{DD1} (pin 24)	4.5	–	5.5	V
V_{DD2} (pin 13)	10.8	–	13.2	V

The following characteristics apply at T_{amb} = 25 °C, V_{DD1} = 5 V, V_{DD2} = 12 V unless otherwise stated.

Supply current

I_{DD1} } Average current with analogues at reset	–	20	40	mA
I_{DD2} }	–	10	20	mA

Analogue rate of change control (pin 12)

Time for any analogue output to change from reset position (mid-point) to end stop with pin 12 connected to V_{SS}	–	3.2	–	s

		min.	typ.	max.	
Oscillator					
Resistor between pins 18 and 19, capacitor between pin 19 and V_{SS}, R = 27 kΩ, C = 27 pF					
Operating frequency		0.8	1.0	1.2	MHz
Used as an amplifier (pin 18 open-circuit)					
Operating frequency		0.8	–	1.2	MHz
Input voltage; HIGH	V_{IH}	4.0	–	V_{DD1}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Inputs					
Data input (pin 22, Schmitt Trigger)					
Input voltage; HIGH	V_{IH}	3.8	–	V_{DD1}	V
Input voltage; LOW	V_{IL}	0	–	1.7	V
Applied voltage (R_{source} = 2 kΩ)		0	–	13.5	V
Input leakage (V_{in} = 5.5 V)		–	–	50	μA
Local reset (pin 2)					
Input voltage; HIGH	V_{IH}	2.5	–	V_{DD1}	V
Input voltage; LOW	V_{IL}	0	–	0.7	V
Input leakage (V_{in} = 5.5 V)		–	–	10	μA
Picture on sense (pin 17)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD1}	V
Input voltage; LOW	V_{iL}	0	–	0.8	V
Applied voltage (R_{source} = 2 kΩ)		0	–	13.5	V
Input leakage (V_{in} = 5.5 V)		–	–	10	μA
Analogue change inhibit (V_{DD2} pin 13)					
Input level for analogues; inhibited		–	–	0.8	V
Input level for analogues; enabled		4.0	–	–	V
Outputs					
Step, Clear and Mute (pins 3, 4 and 9)					
Output voltage; LOW (I_{OL} = 2 mA)	V_{OL}	–	–	0.5	V
Output current in 'off' state (V_{OH} = 13.5 V)		–	–	50	μA
Data output, DLIM and Clock output (pins 5, 7 and 21)					
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	–	V
Output voltage; LOW (I_{OL} = 1 mA)	V_{OL}	–	–	0.5	V
Data output only					
Leakage current in 'off' state (V_{out} = 0 to 5.5 V)		–	–	10	μA

CHARACTERISTICS (continued)

		min.	typ.	max.	
On/standby (pin 6)					
Output voltage; LOW (I_{OL} = 15 mA)	V_{OL}	–	–	0.25	V
Output current in 'off' state (V_{OH} = 13.5 V)		–	–	100	μA
$\overline{\text{DLEN}}$ (pin 8)					
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	–	V
Output voltage; LOW (I_{OL} = 1 mA)	V_{OL}	–	–	0.5	V
When used as input;					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD1}	V
Input voltage; LOW	V_{IL}	–	–	0.8	V
Analogue outputs (pins 10, 11, **14** and 15)					
Output voltage; LOW (I_{OL} = 2 mA)	V_{OL}	–	–	0.7	V
Output voltage; HIGH (I_{OH} = −2 mA) (see Fig.3)	V_{OH}	8	–	–	V
Output current; HIGH (V_{OH} = 11.0 V)	I_{OH}	−200	–	–	μA
Message received indicator (pin 16)					
Output voltage; LOW (I_{OL} = 10 mA)	V_{OL}	–	–	1.0	V
Output current in 'off' state (V_{OH} = 13.5 V)		–	–	50	μA

APPLICATION DATA

The function is quoted against the corresponding pin number.

This device has 3 basic modes of operation. These are:

TV mode Viewdata mode Teletext mode

The response of the device to an input code will vary according to which mode the device is in at that time. Certain input codes will cause the device to change mode, other codes perform different functions depending on the level of the Picture on sense input. See table 1 for full details.

Pin No.

1. V_{SS} Ground – 0 V

2. **Local reset**

   When this input is connected to 0 V, all four analogue outputs revert to their mid-range position, the 'mute' output switches to the 'unmute' state and the 'on/standby' output switches to the 'on' state, and the mode is set to 'TV'. During the normal operation this input should be connected to V_{DD1} through a suitable resistor.

3. **Step output**

   For the purpose of selection of one out of sixteen TV stations, a clear pulse is generated at pin 4 to set a tuning selection system to station 1. This is followed by an appropriate number of stepping pulses at pin 3 to step the tuning system.See Fig.2 for clear and step pulse details.
   These outputs may be connected together if single wire operation is required.

4. **Clear output**

Output to clear station tuning system. See pin 3 details.

5. **$\overline{\text{Data}}$ output**

This 3-state output provides 7-bit inverted serial data, 5 bits of which is identical to the input command message code, the other two bits control 3 modes (i.e. TV, teletext and viewdata This data contains all the teletext and viewdata control functions and interfaces directly with each system. See Fig.5 for details of the data output waveform and Table 2 for details of the output codes. When the data output is not in use the output switches to high impedance to allow the data line to be used by other circuits.

6. **On/standby output**

This output provides control for TV receiver power supply switching. (HIGH = On; LOW = Standby).
The 'standby' state occurs either on receiving the standby input code (Code 3) or with the application of the V_{DD1} supply.
The 'on' state occurs either by operation of the local reset (See pin 2 details) or on receipt of any of the following codes:

Code 1	- Reset
Code 4	- Transfer to TV mode/on
Codes 18 to 28	- Station select
Code 30	- Transfer to viewdata mode
Code 32	- Transfer to teletext mode

On using a station select code to revert from 'standby' to the 'on' state a delay of nominally 2 seconds occurs before the channel selection signals are produced at the step and clear outputs. This is to allow for slow start TV power supplies.

7. **DLIM**

This is a clocking pulse signal that occurs only during serial data output and is used to clock the data externally. Direct interface to the SAA5040 and SAA5050 teletext circuits is possible. See Fig.5 for timing details.

8. **$\overline{\text{DLEN}}$**

This is a 3-state input/output signal that occurs only during the serial data output and it is used in conjunction with the 'clock output' (pin 21) to clock the data output into the DICS system. See Fig.5 for timing details. Holding the $\overline{\text{DLEN}}$ input low inhibits the sending of a data output code. Whilst an output code is being held, no further input codes will be accepted.

9. **Mute output**

This is a bistable output intended for instant sound muting. It is an open-drain output capable of sinking current to V_{SS}.
On receipt of the mute code (Code 2) the output is taken to V_{SS} and a time period of nominally 750 ms is initiated during which no further response is possible at this output. After this time period the reception of the same code will cause the output to return to the HIGH state and a similar immunity time period initiated.
The mute output also goes LOW whilst a programme selection command is being executed and whilst the two second delay after the standby state is in operation.

Pin No. (continued)

10. **Analogue 1 output**

This output provides a variable mark-space ratio waveform, adjustable over 62 values (see Fig.3). When integrated this output provides a d.c. voltage level controllable from approximately 0 to 12 volts which may be used for controlling any of the TV analogue functions. Reception of the AN1+(Code 9) command causes the mark-space ratio to increase, and the AN1−(Code 10) causes the ratio to decrease. The reset function (local or remote) sets the output to approximately a 50% duty cycle.

11. **Analogue 2 output**

This provides a similar output to analogue 1 (pin 10). It is controlled by the AN2+ and AN2− commands (Codes 11 and 12).

12. **Analogue rate of change control**

When this pin is connected to V_{SS} the internal timing chain operating from the oscillator dictates the analogue rate of change, (all four analogues have the same rate of change). The rate under these circumstances is nominally 107 ms/step. By connecting one capacitor and one resistor to this pin as shown on Fig.1 the analogue rate of change is variable from nominally 250 ms/step to 50 ms/step by using a 100 nF capacitor and a resistor in the range 470 kΩ to 2,2 MΩ.

13. V_{DD2} +12 V Supply

This supply feeds the analogue output stages only and does not affect the logic section of the circuit and therefore it may be removed at any time. The analogue outputs will cease but will restart with the same mark-space ratio when the supply is re-applied provided that the V_{DD1} supply has been maintained. Whilst the V_{DD2} supply is removed all commands that change analogue mark-space ratios are ignored.

14. **Analogue 3 output**

This provides a similar output to analogue 1 (pin 10). It is controlled by the AN3+ and AN3− (Codes 13 and 14). If the SAA5010 is in the teletext or viewdata modes the codes will control the mark-space ratio only if the Picture on sense input (pin 17) is high.

15. **Analogue 4 output**

See description of analogue 3 output (pin 14). This output is controlled by codes 15 and 16.

16. **Message received indicator**

This is an open drain output and is capable of sinking current to V_{SS} when a correct input data sequence has been received. The output remains low while the input signal is present and will revert to the high state after a period of silence of about 64 ms at the input. This output is capable of driving a LED display directly.

17. **Picture on sense**

When in teletext or viewdata modes, analogues 3 and 4 will be controlled by commands 13 to 16 only if this input is high (see tables 1 and 2).

18, 19. **Oscillator timing components**

A resistor and capacitor are required to time the oscillator which controls the timing of all the internal functions of the circuit. The capacitor is connected between pins 19 and 1 and the resistor between pins 18 and 19.

20. **Teledata modes inhibit**

This input when connected to V_{DD1} inhibits both the teletext and viewdata modes, thus permitting sets not equipped with these features to specifically exclude these modes. If these modes are required this input should be connected to V_{SS}.

21. **Clock output**

This is a 1:1 mark-space ratio clocking pulse of nominal frequency 62.5 kHz, and is intended for control to the DICS system. For phase locking purposes a divide by four must be used between the DICS system 4 MHz oscillator and pin 19.

22. **Data input**

The 24-bit message code must be applied to this input either from a pulse retrieving circuit driven by a transmission system or from the output of a local keyboard system. The SAA5000 generates the required data sequence. (See Fig 4 for details of data input format).

23. **Data input type selector**

By connecting this input to V_{SS} the input data is expected to be from an ultrasonic transmission system, and with this input connected to V_{DD1} the data is expected to be from an infra-red transmission system. For details of the expected pulse format see the SAA5000 data sheet.

24. V_{DD1} +5 V supply

This is the power supply input for the logic section of the circuit and must remain supplied during the standby condition.

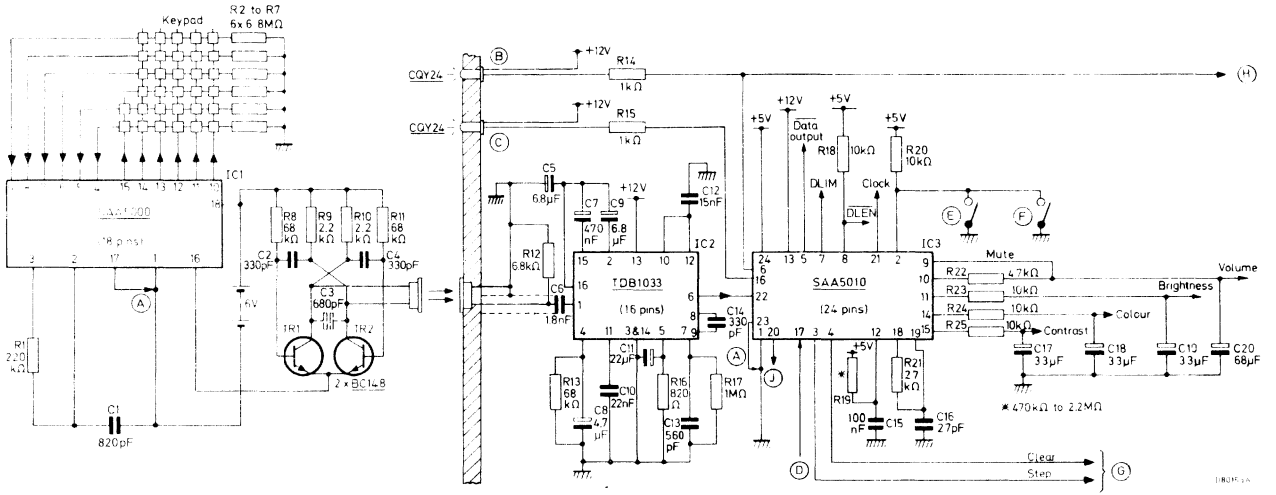


Fig.1 Ultrasonic System

A. Ultrasonic/infrared selection
B. On/standby indicator
C. Message received indicator
D. 'Picture on' input
E. Local reset switch
F. Third mains switch contact pair
G. To touch tuner
H. On/standby control
J. Mode selection

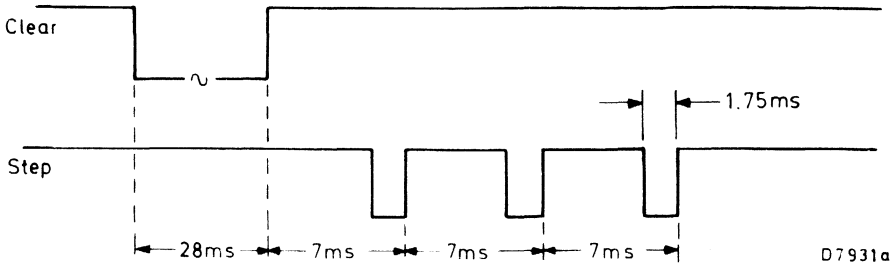


Fig. 2 Outputs to channel selector to select CHANNEL 4.

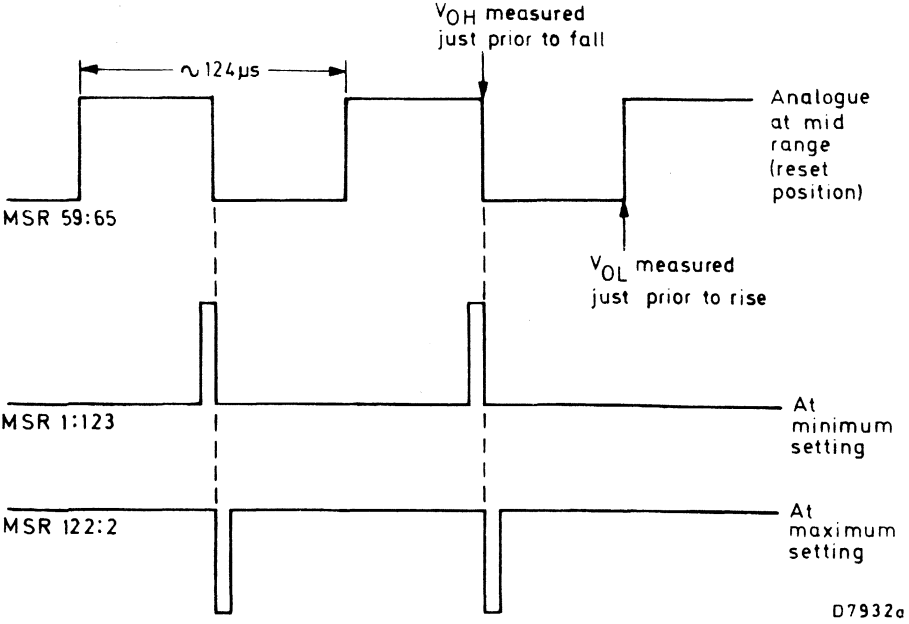


Fig. 3 Analogue output waveforms.

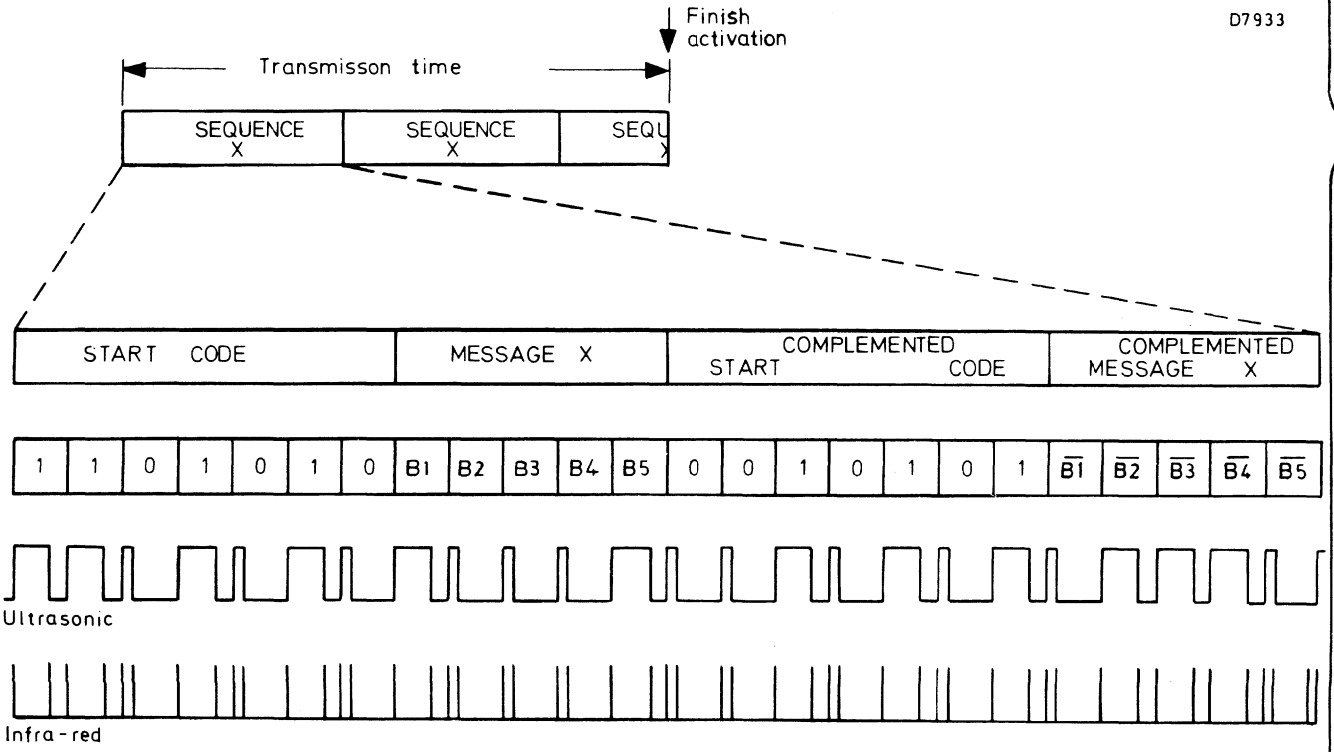


Fig. 4 Input data waveforms.

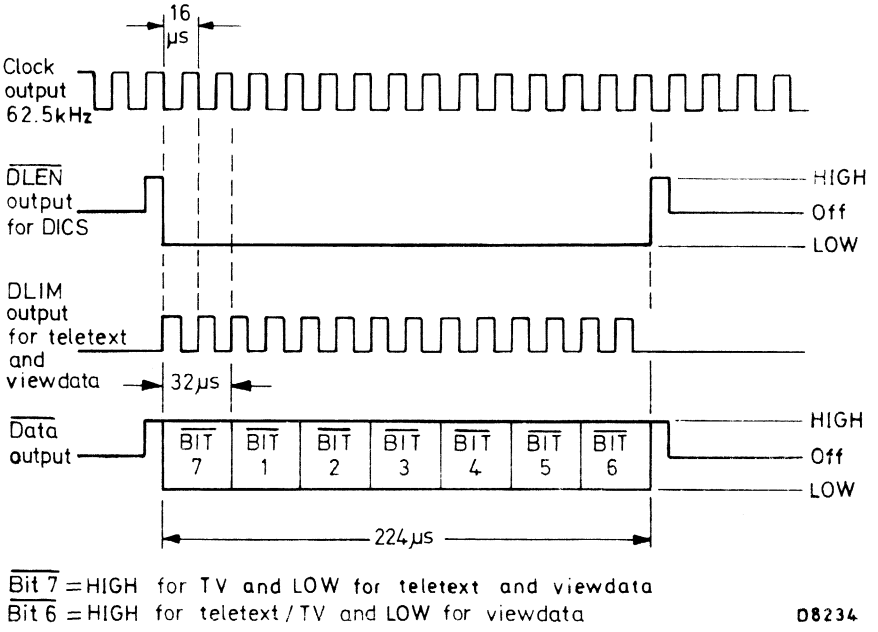


Fig. 5 Data output and clock output waveforms.

	Code received					MODE				
	B5	B4	B3	B2	B1	TV	Teletext (Pin 17 LOW)	Teletext (Pin 17 HIGH)	Viewdata (Pin 17 LOW)	Viewdata (Pin 17 HIGH)
1	0	0	0	0	0	Reset/on	Transfer to TV/reset	Transfer to TV/reset	Transfer to TV/reset	Transfer to TV/reset
2	0	0	0	0	1	Mute	Mute	Mute	Mute	Mute
3	0	0	0	1	0	Standby	Transfer to TV/standby	Transfer to TV/standby	Transfer to TV/standby	Transfer to TV/standby
4	0	0	0	1	1	On	Transfer to TV	Transfer to TV	Transfer to TV	Transfer to TV
5	0	0	1	0	0	–	–	–	–	–
6	0	0	1	0	1	–	–	–	–	–
7	0	0	1	1	0	1 ✱ (1)	–	–	–	–
8	0	0	1	1	1	–	–	–	–	–
9	0	1	0	0	0	Analogue 1+	Analogue 1+	Analogue 1+	Analogue 1+	Analogue 1+
10	0	1	0	0	1	Analogue 1–	Analogue 1–	Analogue 1–	Analogue 1–	Analogue 1–
11	0	1	0	1	0	Analogue 2+	Analogue 2+	Analogue 2+	Analogue 2+	Analogue 2+
12	0	1	0	1	1	Analogue 2–	Analogue 2–	Analogue 2–	Analogue 2–	Analogue 2–
13	0	1	1	0	0	Analogue 3+	–	Analogue 3+	–	Analogue 3+
14	0	1	1	0	1	Analogue 3–	–	Analogue 3–	–	Analogue 3–
15	0	1	1	1	0	Analogue 4+	–	Analogue 4+	–	Analogue 4+
16	0	1	1	1	1	Analogue 4–	–	Analogue 4–	–	Analogue 4–
17	1	0	0	0	0	Programme 1/on	–	–	–	–
18	1	0	0	0	1	Programme 2/on	–	–	–	–
19	1	0	0	1	0	Programme 3/on	–	–	–	–
20	1	0	0	1	1	Programme 4/on	–	–	–	–
21	1	0	1	0	0	Programme 5/on	–	–	–	–
22	1	0	1	0	1	Programme 6/on	–	–	–	–
23	1	0	1	1	0	Programme 7/on	–	–	–	–
24	1	0	1	1	1	Programme 8/on	–	–	–	–
25	1	1	0	0	0	Programme 9/on	–	–	–	–
26	1	1	0	0	1	Programme 10/on	–	–	–	–
27	1	1	0	1	0	Programme 11/on	–	–	–	–
28	1	1	0	1	1	Programme 12/on	–	–	–	–
29	1	1	1	0	0	–	–	–	–	–
30	1	1	1	0	1	Transfer to viewdata/on	Transfer to viewdata	Transfer to viewdata	–	–
31	1	1	1	1	0	Transfer to teletext (2)	–	–	Transfer to teletext	Transfer to teletext
32	1	1	1	1	1	Transfer to teletext/on	–	–	Transfer to teletext	Transfer to teletext

Blank entries indicate those codes for which the only device function is a possible transmission on the Data outputs (See Table 2)

TABLE 1: Input code responses

Notes. (1) This code is used before codes 17 to 22 to select programmes 11 to 16 (programmes 11 and 12 may also be selected by using codes 27 and 28).

(2) This transfer to teletext mode does not occur if on/standby output is low.

	Code received					MODE								
						TV			Teletext			Viewdata		
	B5	B4	B3	B2	B1	B7	B6	Repetition frequency of output	B7	B6	Repetition frequency of output	B7	B6	Repetition frequency of output
1	0	0	0	0	0	0	0	S			NT			NT
2	0	0	0	0	1	0	0	S	1	0	S	1	1	S
3	0	0	0	1	0	0	0	S			NT			NT
4	0	0	0	1	1	0	0	S			NT			NT
5	0	0	1	0	0	0	0	S	1	0	S	1	1	S
6	0	0	1	0	1	0	0	S	1	0	S	1	1	S
7	0	0	1	1	0	0	0	S	1	0	R100	1	1	R100
8	0	0	1	1	1	0	0	S	1	0	R100	1	1	R100
9	0	1	0	0	0			NT			NT			NT
10	0	1	0	0	1			NT			NT			NT
11	0	1	0	1	0			NT			NT			NT
12	0	1	0	1	1			NT			NT			NT
13	0	1	1	0	0			NT	1	0	S (3)	1	1	S (3)
14	0	1	1	0	1			NT	1	0	S (3)	1	1	S (3)
15	0	1	1	1	0			NT	1	0	S (3)	1	1	S (3)
16	0	1	1	1	1			NT	1	0	S (3)	1	1	S (3)
17	1	0	0	0	0	0	0	S	1	0	S	1	1	S
18	1	0	0	0	1	0	0	S	1	0	S	1	1	S
19	1	0	0	1	0	0	0	S	1	0	S	1	1	S
20	1	0	0	1	1	0	0	S	1	0	S	1	1	S
21	1	0	1	0	0	0	0	S	1	0	S	1	1	S
22	1	0	1	0	1	0	0	S	1	0	S	1	1	S
23	1	0	1	1	0	0	0	S	1	0	S	1	1	S
24	1	0	1	1	1	0	0	S	1	0	S	1	1	S
25	1	1	0	0	0	0	0	S	1	0	S	1	1	S
26	1	1	0	0	1	0	0	S	1	0	S	1	1	S
27	1	1	0	1	0	0	0	S	1	0	S	1	1	S
28	1	1	0	1	1	0	0	S	1	0	S	1	1	S
29	1	1	1	0	0			NT	1	0	S	1	1	S
30	1	1	1	0	1	0	0	S (2)			NT	1	1	S
31	1	1	1	1	0	0	0	S (1)	1	0	S			NT
32	1	1	1	1	1	0	0	S (2)	1	0	S			NT

TABLE 2: Data output codes

(1) This code is NT if Teledata inhibit is low and on/standby output is high.

(2) These codes are NT if Teledata inhibit is low.

(3) These codes are NT if Picture on sense input is high.

Key to symbols: NT = Not transmitted

S = Single transmission

R100 = Repeated approximately every 100 ms.

Note

Table shows logic output of B6 and B7, $\overline{B6}$ and $\overline{B7}$ are transmitted.

B1 to B5 are as received input, $\overline{B1}$ to $\overline{B5}$ are transmitted.

REMOTE CONTROL RECEIVER DECODER

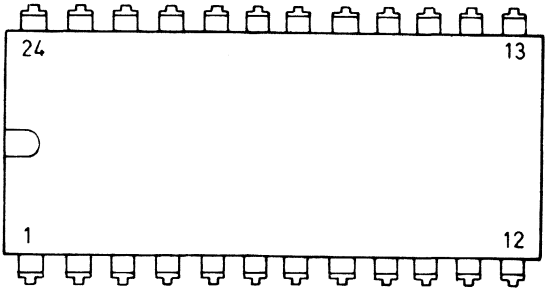
The SAA5012A is a MOS N-channel integrated circuit which provides the receiver decoding function for the remote control of television receivers.
The SAA5012A is a 24-lead device for the control of television receivers incorporating binary addressable tuning selector systems and including those equipped with teletext and viewdata facilities. It is suitable for use either in ultrasonic or infra-red transmission systems and is intended for use with the SAA5000 transmitter encoder integrated circuit. The SAA5012A is also suitable for direct connection to the SAA5040 series and the SAA5050 series teletext decoder circuits.

QUICK REFERENCE DATA

Supply voltage				
Digital	V_{DD1}	nom.	5	V
Analogue	V_{DD2}	nom.	12	V
Supply current				
Digital	I_{DD1}	typ.	20	mA
Analogue	I_{DD2}	typ.	10	mA
Operating temperature range	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT−101A)



Viewed from top

PINNING

1 - V_{SS}
2 - Local reset
3 - Counter output A (L.S.B.)
4 - Counter output B
5 - $\overline{\text{DATA}}$ out
6 - On/standby
7 - DLIM
8 - Counter output C
9 - Mute
10 - Analogue 1
11 - Analogue 2
12 - Analogue rate of change control
13 - V_{DD2}
14 - Analogue 3
15 - Analogue 4
16 - Message received indicator
17 - Picture on sense
18 - Oscillator (R connection)
19 - Oscillator (C and R common connection)
20 - Teledata modes inhibit/counter step
21 - Counter output D (M.S.B.)
22 - Data input
23 - Data input type selector
24 - V_{DD1}

DESCRIPTION

The data input is in the form of a 7-bit framing code and a 5-bit message followed by an identical but complemented sequence making a complete 24-bit message sequence. Error checking is effected within the device to ensure a high degree of corrupted signal immunity. The SAA5012A allows for 12 channel selections, 4 analogue functions (e.g. volume, contrast, brightness and saturation), sound muting, and 'set in standby' to be controlled remotely. An output is provided to drive visual and/or audible indication of a received code. Logic outputs are available to provide control data and clocks for use in teletext and viewdata systems. No adjustments or critical components are required in the peripheral circuitry.

Note: Use of the local stepping facility (Pin 20), increases the number of possible channel selections to 16.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See MOS Handling Notes).

RATINGS

Limiting values of operation in accordance with the Absolute Maximum System.

Voltages (with respect to pin 1)		min.	max.	
Supply voltage (pin 24)	V_{DD1}	−0.3	7.5	V
(pin 13)	V_{DD2}	−0.3	14	V
Input voltages All inputs except Data in and Picture on sense (pins 2, 12, 18, 19, 20, 23)		−0.3	7.5	V
Data in and Picture on sense (pins 22, 17)		−0.3	14	V
Output voltage All outputs to TV functions (pins 6, 9, 10, 11, 14, 15, 16)		−0.3	14	V
Logic outputs (pins 3, 4, 5, 7, 8, 21)		−0.3	7.5	V

Temperatures			
Storage temperature	T_{stg}	−20 to +125	°C
Operating ambient temperature	T_{amb}	−20 to +70	°C

CHARACTERISTICS

Supply voltages	min.	typ.	max.	
V_{DD1} (pin 24)	4.5	–	5.5	V
V_{DD2} (pin 13)	10.8	–	13.2	V

The following characteristics apply at T_{amb} = 25 °C, V_{DD1} = 5 V, V_{DD2} = 12 V unless otherwise stated.

Supply current				
I_{DD1} Average current with analogues at reset	–	20	40	mA
I_{DD2} Average current with analogues at reset	–	10	20	mA

Analogue rate of change control (pin 12)				
Time for any analogue output to change from reset position (mid-point) to end stop with pin 12 connected to V_{SS}.	–	3.2	–	s

Oscillator		min.	typ.	max.	
Resistor between pins 18 and 19, capacitor between pin 19 and V_{SS}, R = 27 kΩ, C = 27 pF					
Operating frequency		0.8	1.0	1.2	MHz
Used as an amplifier (pin 18 open-circuit)					
Operating frequency		0.8	–	1.2	MHz
Input voltage; HIGH	V_{IH}	4.0	–	V_{DD1}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Inputs					
Data input (pin 22, Schmitt Trigger)					
Input voltage; HIGH	V_{IH}	3.8	–	V_{DD2}	V
Input voltage; LOW	V_{IL}	0	–	1.7	V
Applied voltage (R_{source} = 2 kΩ)		0	–	13.5	V
Input leakage (V_{in} = 5.5 V)		–	–	50	μA
Local reset (pin 2)					
Input voltage; HIGH	V_{IH}	2.5	–	V_{DD1}	V
Input voltage; LOW	V_{IL}	0	–	0.7	V
Input leakage (V_{in} = 5.5 V)		–	–	10	μA
Picture on sense (pin 17)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD2}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Applied voltage (R_{source} = 2 kΩ)		0	–	13.5	V
Input leakage (V_{in} = 5.5 V)		–	–	10	μA
Analogue change inhibit (V_{DD2} pin 13)					
Input level for analogues; inhibited		–	–	0.8	V
Input level for analogues; enabled		4.0	–	–	V
Teledata inhibit/counter step (pin 20)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD1}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input leakage (V_{in} = 5.5 V)		–	–	10	μA
Outputs					
Mute (pin 9)					
Output voltage; LOW (I_{OL} = 2 mA)	V_{OL}	–	–	0.5	V
Output current in 'off' state (V_{OH} = 13.5 V)		–	–	50	μA
$\overline{\text{DATA}}$ output, **and DLIM** (pins 5, 7)					
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	–	V
Output voltage; LOW (I_{OL} = 1 mA)	V_{OL}	–	–	0.5	V
$\overline{\text{DATA}}$ **output** only					
Leakage current in 'off' state (V_{out} = 0 to 5.5 V)		–	–	10	μA

CHARACTERISTICS (continued)			min.	typ.	max.	
Counter outputs (pins 3, 4, 8, 21)						
Output voltage; LOW (I_{OL} = 1 mA)		V_{OL}	–	–	0.5	V
Output current in 'off' state (V_{OH} = 5.5 V)			–	–	50	μA
On/standby (pin 6)						
Output voltage; LOW (I_{OL} = 15 mA)		V_{OL}	–	–	0.25	V
Output current in 'off' state (V_{OH} = 13.5 V)			–	–	100	μA
Analogue outputs (pins 10, 11, 14 and 15)						
Output voltage; LOW (I_{OL} = 2 mA)	(see Fig.3)	V_{OL}	–	–	0.7	V
Output voltage; HIGH (I_{OH} = −2 mA)	(see Fig.3)	V_{OH}	8	–	–	V
Output current; HIGH (V_{OH} = 11.0 V)	(see Fig.3)	I_{OH}	−200	–	–	μA
Message received indicator (pin 16)						
Output voltage; LOW (I_{OL} = 10 mA)		V_{OL}	–	–	1.0	V
Output current in 'off' state (V_{OH} = 13.5 V)			–	–	50	μA

APPLICATION DATA

The function is quoted against the corresponding pin number.

This device has 3 basic modes of operation. These are:

TV mode Viewdata mode Teletext mode

The response of the device to an input code will vary according to which mode the device is in at that time. Certain input codes will cause the device to change mode, other codes perform different functions depending on the level of the Picture on sense input. See table 1 for full details.

Pin No.

1. V_{SS} Ground – 0 V

2. **Local reset**

   When this input is connected to 0 V, all four analogue outputs revert to their mid-range position, the 'mute' output switches to the 'unmute' state and the 'on/standby' output switches to the 'on' state, and the mode is set to 'TV'. During the normal operation this input should be connected to V_{DD1} through a suitable resistor. This input is also used to control the direction of the counter stepping (see pin 20 details).

3. **Counter output A** (L.S.B.)

   For the purpose of selection of one out of sixteen TV stations, this latched output provides the least significant bit of a four-bit binary output (Bit 1). It is an open drain output capable of sinking current to V_{SS}. (See Fig.2)

4. **Counter output B**

   For the purpose of selection of one out of sixteen TV stations, this latched output provides bit 2 of the four-bit binary output. It is an open drain output capable of sinking current to V_{SS}. (See Fig.2).

5. $\overline{\text{DATA}}$ output

This 3-state output provides 7-bit inverted serial data, 5 bits of which is identical to the input command message code, the other two bits control 3 modes (i.e. TV, teletext and viewdata). This data contains all the teletext and viewdata control functions and interfaces directly with each system. See Fig.5 for details of the data output waveform and Table 2 for details of the output codes. When the data output is not in use the output switches to high impedance to allow the data line to be used by other circuits.

6. On/standby output

This output provides control for TV receiver power supply switching. (HIGH = On; LOW = Standby).
The 'standby' state occurs either on receiving the standby input code (Code 3) or with the application of the V_{DD1} supply.
The 'on' state occurs either by operation of the local reset (See pin 2 details) or on receipt of any of the following codes:

Code 1	- Reset
Code 4	- Transfer to TV mode/on
Codes 18 to 28	- Station select
Code 30	- Transfer to viewdata mode
Code 32	- Transfer to teletext mode

On using a station select code to revert from 'standby' to the 'on' state a delay of nominally 2 seconds occurs before the $\overline{\text{DATA}}$ out and DLIM signals are produced. The mute output goes LOW during this time. This is to allow for slow start TV power supplies.

7. DLIM

This is a clocking pulse signal that occurs only during serial data output and is used to clock the data externally. Direct interface to the SAA5040 and SAA5050 teletext circuits is possible. See Fig.5 for timing details.

8. Counter output C

For the purpose of selection of one of sixteen TV stations this latched output provides bit 3 of the four-bit binary output. It is an open drain output capable of sinking current to V_{SS}. (See Fig.2).

9. Mute output

This is a bistable output intended for instant sound muting. It is an open-drain output capable of sinking current to V_{SS}.
On receipt of the mute code (Code 2) the output is taken to V_{SS} and a time period of nominally 750 ms is initiated during which no further response is possible at this output. After this time period the reception of the same code will cause the output to return to the HIGH state and a similar immunity time period initiated.
The mute output also goes LOW whilst a remote programme selection command is being executed and whilst the two second delay after the standby state is in operation.

Pin No. (continued)

10. **Analogue 1 output**

This output provides a variable mark-space ratio waveform, adjustable over 62 values (see Fig.3). When integrated this output provides a d.c. voltage level controllable from approximately 0 to 12 volts which may be used for controlling any of the TV analogue functions. Reception of the AN1+(Code 9) command causes the mark-space ratio to increase, and the AN1−(Code 10) causes the ratio to decrease. The reset function (local or remote) sets the output to approximately a 50% duty cycle.

11. **Analogue 2 output**

This provides a similar output to analogue 1 (pin 10). It is controlled by the AN2+ and AN2− commands (Codes 11 and 12).

12. **Analogue rate of change control**

When this pin is connected to V_{SS} the internal timing chain operating from the oscillator dictates the analogue rate of change, (all four analogues have the same rate of change). The rate under these circumstances is nominally 107 ms/step. By connecting one capacitor and one resistor to this pin as shown on Fig.1 the analogue rate of change is variable from nominally 250 ms/step to 50 ms/step by using a 100 nF capacitor and a resistor in the range 2.2 MΩ to 470 kΩ.

13. V_{DD2} +12 V Supply

This supply feeds the analogue output stages only and does not affect the logic section of the circuit and therefore it may be removed at any time. The analogue outputs will cease but will restart with the same mark-space ratio when the supply is re-applied provided that the V_{DD1} supply has been maintained. Whilst the V_{DD2} supply is removed all commands that change analogue mark-space ratios are ignored.

14. **Analogue 3 output**

This provides a similar output to analogue 1 (pin 10). It is controlled by the AN3+ and AN3− commands (Codes 13 and 14). If the SAA5012A is in the teletext or viewdata modes the codes will control the mark-space ratio only if the Picture on sense input (pin 17) is high.

15. **Analogue 4 output**

See description of analogue 3 output (pin 14). This output is controlled by codes 15 and 16.

16. **Message received indicator**

This is an open drain output and is capable of sinking current to V_{SS} when a correct input data sequence has been received. The output remains low while the input signal is present and will revert to the high state after a period of silence of about 64 ms at the input. This output is capable of driving a LED display directly.

17. **Picture on sense**

When in teletext or viewdata modes, analogues 3 and 4 will be controlled by commands 13 to 16 only if this input is high (see tables 1 and 2).

18, 19. **Oscillator timing components**

A resistor and capacitor are required to time the oscillator which controls the timing of all the internal functions of the circuit. The capacitor is connected between pins 19 and 1 and the resistor between pins 18 and 19. The SAA5012A may be driven by an external clock applied to pin 19. In this case pin 18 must be left open circuit.

20. **Teledata modes inhibit/counter step**

This is a dual purpose input. When the input is held HIGH it inhibits both the teletext and viewdata modes, thus permitting sets not equipped with these features to specifically exclude these modes. If these modes are required this input should be held LOW. The other purpose of this input is to provide a local stepping facility for the internal tuning selection counter. This is intended for emergency use when the remote control handset is not available. In order to step the counter this input should be pulsed into the opposite state from which it is normally held. Each local stepping pulse will cause the counter to change. It will count down if pin 2 is HIGH, and up if pin 2 is LOW. Data output codes and the sound mute pulse are not sent during local stepping, but during "step-up" the local reset conditions apply. (See pin 2 details).

21. **Counter output D (M.S.B.)**

For the purpose of selection of one out of sixteen TV stations this latched output provides the most significant bit of a four-bit binary output. It is an open drain coutput capable of sinking current to V_{SS}. (See Fig.2)

22. **Data input**

The 24-bit message code must be applied to this input either from a pulse retrieving circuit driven by a transmission system or from the output of a local keyboard system. The SAA5000 generates the required data sequence. (See Fig.4 for details of data input format).

23. **Data input type selector**

By connecting this input to V_{SS} the input data is expected to be from an ultrasonic transmission system, and with this input connected to V_{DD1} the data is expected to be from an infra-red transmission system. For details of the expected pulse format see the SAA5000 data sheet.

24. V_{DD1} +5 V supply

This is the power supply input for the logic section and must remain supplied during the standby condition.

PERIPHERAL CIRCUITRY

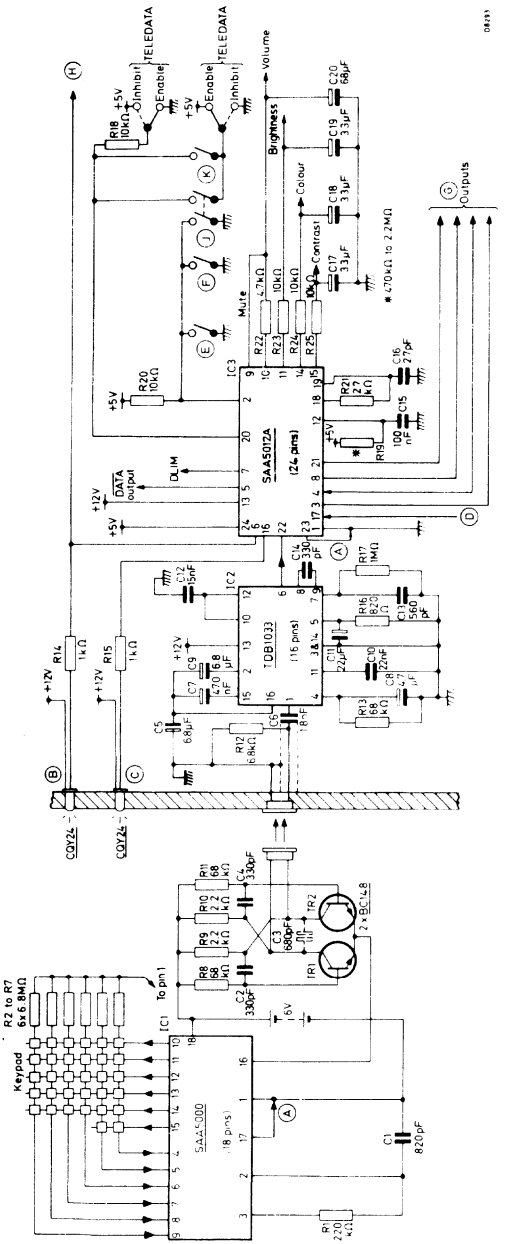


Fig.1 Ultrasonic System

A. Ultrasonic/infrared selection
B. On/standby indicator
C. Message received indicator
D. 'Picture on' input
E. Local reset switch
F. Third mains switch contact pair
G. Counter outputs to tuning system.
H. On/standby control
J. Counter step up
K. Counter step down.

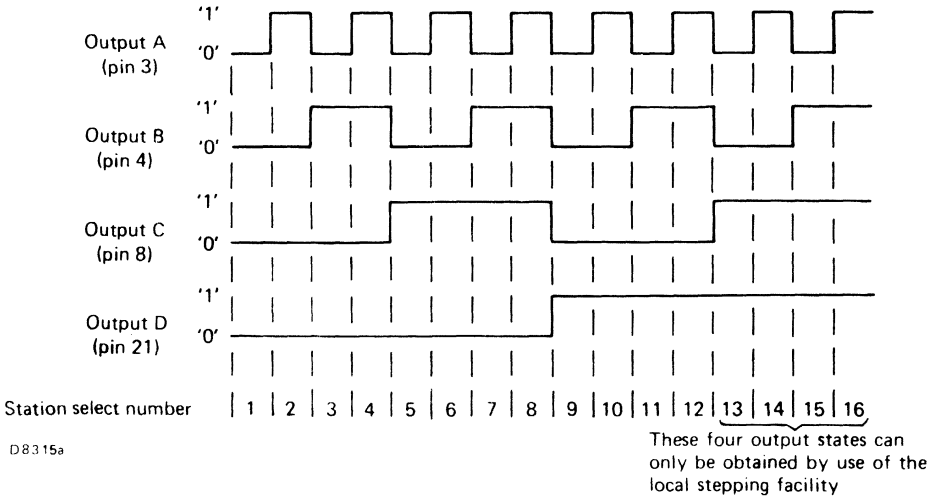


Fig.2 Counter outputs

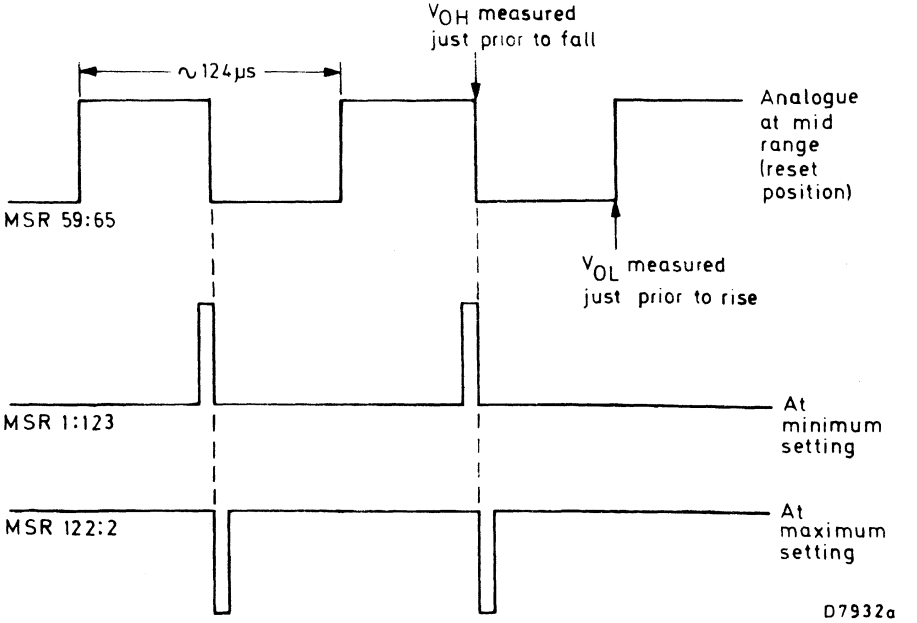


Fig.3 Analogue output waveforms

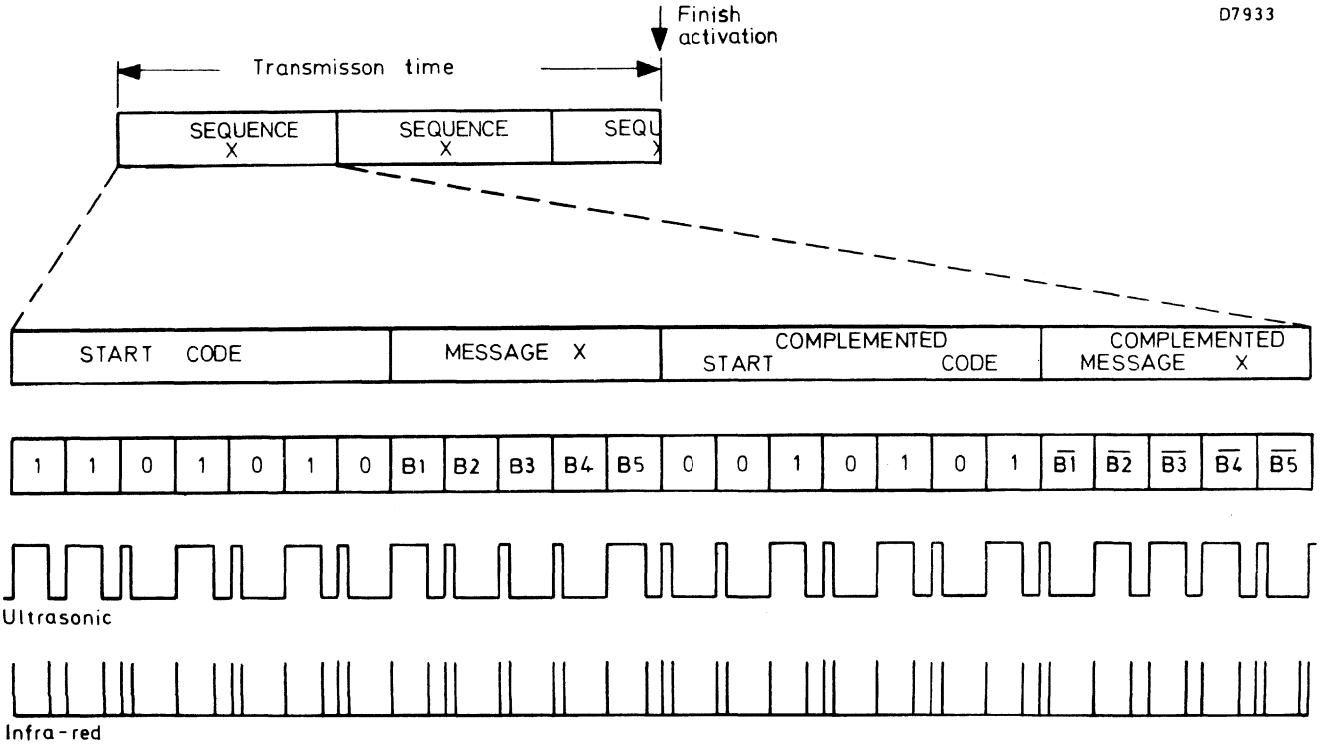


Fig.4 Input data waveforms

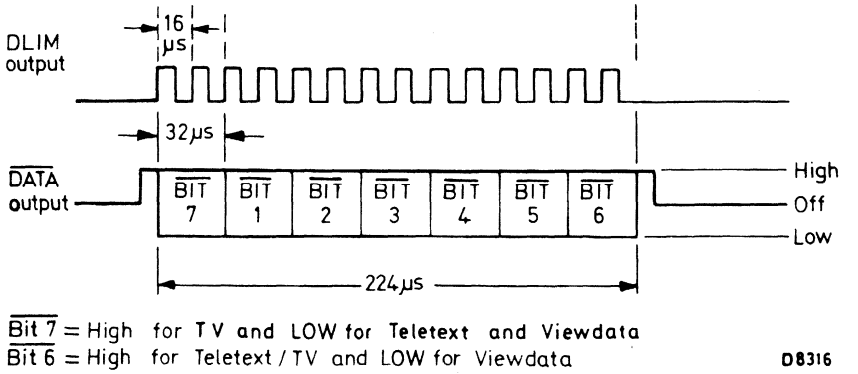


Fig.5 $\overline{\text{DATA}}$ output and DLIM output waveforms

	Code received					MODE				
	B5	B4	B3	B2	B1	TV	Teletext (Pin 17 LOW)	Teletext (Pin 17 HIGH)	Viewdata (Pin 17 LOW)	Viewdata (Pin 17 HIGH)
1	0	0	0	0	0	Reset/on	Transfer to TV/reset	Transfer to TV/reset	Transfer to TV/reset	Transfer to TV/reset
2	0	0	0	0	1	Mute	Mute	Mute	Mute	Mute
3	0	0	0	1	0	Standby	Transfer to TV/standby	Transfer to TV/standby	Transfer to TV/standby	Transfer to TV/standby
4	0	0	0	1	1	On	Transfer to TV	Transfer to TV	Transfer to TV	Transfer to TV
5	0	0	1	0	0	—	—	—	—	—
6	0	0	1	0	1	—	—	—	—	—
7	0	0	1	1	0	—	—	—	—	—
8	0	0	1	1	1	—	—	—	—	—
9	0	1	0	0	0	Analogue 1+	Analogue 1+	Analogue 1+	Analogue 1+	Analogue 1+
10	0	1	0	0	1	Analogue 1–	Analogue 1–	Analogue 1–	Analogue 1–	Analogue 1–
11	0	1	0	1	0	Analogue 2+	Analogue 2+	Analogue 2+	Analogue 2+	Analogue 2+
12	0	1	0	1	1	Analogue 2–	Analogue 2–	Analogue 2–	Analogue 2–	Analogue 2–
13	0	1	1	0	0	Analogue 3+	—	Analogue 3+	—	Analogue 3+
14	0	1	1	0	1	Analogue 3–	—	Analogue 3–	—	Analogue 3–
15	0	1	1	1	0	Analogue 4+	—	Analogue 4+	—	Analogue 4+
16	0	1	1	1	1	Analogue 4–	—	Analogue 4–	—	Analogue 4–
17	1	0	0	0	0	Programme 1/on	—	—	—	—
18	1	0	0	0	1	Programme 2/on	—	—	—	—
19	1	0	0	1	0	Programme 3/on	—	—	—	—
20	1	0	0	1	1	Programme 4/on	—	—	—	—
21	1	0	1	0	0	Programme 5/on	—	—	—	—
22	1	0	1	0	1	Programme 6/on	—	—	—	—
23	1	0	1	1	0	Programme 7/on	—	—	—	—
24	1	0	1	1	1	Programme 8/on	—	—	—	—
25	1	1	0	0	0	Programme 9/on	—	—	—	—
26	1	1	0	0	1	Programme 10/on	—	—	—	—
27	1	1	0	1	0	Programme 11/on	—	—	—	—
28	1	1	0	1	1	Programme 12/on	—	—	—	—
29	1	1	1	0	0	—	—	—	—	—
30	1	1	1	0	1	Transfer to viewdata/on	Transfer to viewdata	Transfer to viewdata	—	—
31	1	1	1	1	0	Transfer to teletext *	—	—	Transfer to teletext	Transfer to teletext
32	1	1	1	1	1	Transfer to teletext/on	—	—	Transfer to teletext	Transfer to teletext

Blank entries indicate those codes for which the only device function is a possible transmission on the Data outputs (See Table 2)

TABLE 1: Input code responses

*This transfer to teletext mode does not occur if on/standby output is low.

	Code received					MODE								
						TV			Teletext			Viewdata		
	B5	B4	B3	B2	B1	B7	B6	Repetition frequency of output	B7	B6	Repetition frequency of output	B7	B6	Repetition frequency of output
1	0	0	0	0	0	0	0	S			NT			NT
2	0	0	0	0	1	0	0	S	1	0	S	1	1	S
3	0	0	0	1	0	0	0	S			NT			NT
4	0	0	0	1	1	0	0	S			NT			NT
5	0	0	1	0	0	0	0	S	1	0	S	1	1	S
6	0	0	1	0	1	0	0	S	1	0	S	1	1	S
7	0	0	1	1	0	0	0	S	1	0	R100	1	1	R100
8	0	0	1	1	1	0	0	S	1	0	R100	1	1	R100
9	0	1	0	0	0			NT			NT			NT
10	0	1	0	0	1			NT			NT			NT
11	0	1	0	1	0			NT			NT			NT
12	0	1	0	1	1			NT			NT			NT
13	0	1	1	0	0			NT	1	0	S (3)	1	1	S (3)
14	0	1	1	0	1			NT	1	0	S (3)	1	1	S (3)
15	0	1	1	1	0			NT	1	0	S (3)	1	1	S (3)
16	0	1	1	1	1			NT	1	0	S (3)	1	1	S (3)
17	1	0	0	0	0	0	0	S	1	0	S	1	1	S
18	1	0	0	0	1	0	0	S	1	0	S	1	1	S
19	1	0	0	1	0	0	0	S	1	0	S	1	1	S
20	1	0	0	1	1	0	0	S	1	0	S	1	1	S
21	1	0	1	0	0	0	0	S	1	0	S	1	1	S
22	1	0	1	0	1	0	0	S	1	0	S	1	1	S
23	1	0	1	1	0	0	0	S	1	0	S	1	1	S
24	1	0	1	1	1	0	0	S	1	0	S	1	1	S
25	1	1	0	0	0	0	0	S	1	0	S	1	1	S
26	1	1	0	0	1	0	0	S	1	0	S	1	1	S
27	1	1	0	1	0	0	0	S	1	0	S	1	1	S
28	1	1	0	1	1	0	0	S	1	0	S	1	1	S
29	1	1	1	0	0			NT	1	0	S	1	1	S
30	1	1	1	0	1	0	0	S (2)			NT	1	1	S
31	1	1	1	1	0	0	0	S (1)	1	0	S			NT
32	1	1	1	1	1	0	0	S (2)	1	0	S			NT

TABLE 2: Data output codes

(1) This code is NT if Teledata inhibit is low and on/standby output is high.

(2) These codes are NT if Teledata inhibit is low.

(3) These codes are NT if Picture on sense input is high.

Key to symbols: NT = Not transmitted

S = Single transmission

R100 = Repeated approximately every 100 ms.

Note

Table shows logic output of B6 and B7, $\overline{B6}$ and $\overline{B7}$ are transmitted.

B1 to B5 are as received input, $\overline{B1}$ to $\overline{B5}$ are transmitted.

TELETEXT TIMING CHAIN CIRCUIT

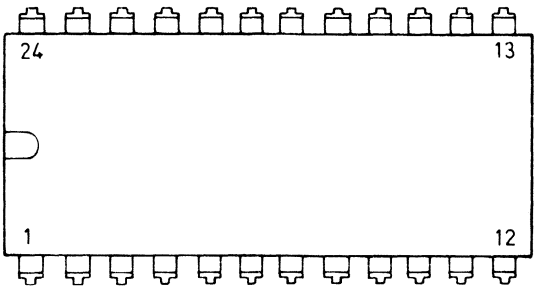
The SAA5020 is an MOS N-channel integrated circuit which performs the timing functions for a teletext system.
The SAA5020 is a 24-lead device which provides the necessary timing signals to the teletext page memory and to the Character Generator (SAA5050). It works in conjunction with the Video Processor Circuit (SAA5030) and the Teletext Acquisition and Control Circuit (SAA5040). The operation of the SAA5020 maintains the synchronisation between the teletext system and the incoming video signal.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom	5	V
Supply current	I_{DD}	typ	20	mA
Operating ambient temperature	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)



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PINNING

1. V_{SS}
2. 6 MHz input (F6)
3. 6 MHz output (TR6)
4. 1 MHz output (F1)
5. 'After Hours' sync ($\overline{AHS}$)
6. Fast line reset (FLR)
7. General line reset ($\overline{GLR}$)
8. Phase lock output ($\overline{PL}$)
9. Colour burst blanking ($\overline{CBB}$)
10. Field sync input (FS)
11. Character rounding select (CRS)
12. V_{DD}
13. Load output shift register enable (LOSE)
14. Data entry window (DEW)
15. Transmitted large character ($\overline{TLC}$)
16. High impedance enable (HIE)
17. Big character select ($\overline{BCS}$)
18. Top/bottom ($\overline{T}$/B)
19. Memory address 0 (A_0)
20. Memory address 1 (A_1)
21. Memory address 2 (A_2)
22. Memory address 3 (A_3)
23. Memory address 4 (A4)
24. Read address clock (RACK)

DESCRIPTION

The basic input to the SAA5020 is a 6 MHz clock signal from the Video Processor Circuit (SAA5030). This clock signal is buffered and is available as an output. A divide-by-six counter produces the character rate of 1 MHz. This is followed by a divide-by-64 to produce the line rate and a further divide by 312/313 to derive the field rate.
The line rate is also divided by 10 to clock a divide-by-24 counter for the teletext memory row addresses. Logic is incorporated to enable the selection of big character display, and to enable the display of transmitted large characters. An output is provided to enable character rounding for normal height characters. A composite sync. signal ($\overline{AHS}$) is available as an output which can be used to synchronise the display time bases.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See MOS Handling Notes).

RATINGS Limiting values in accordance with the Absolute Maximum System.

Voltages (with respect to pin 1)

	min.	max.	
Supply voltage V_{DD} (pin 12)	−0.3	7.5	V
Input voltage All inputs (pins 2, 6, 10, 15, 16, 17, 18)	−0.3	7.5	V
Output voltage (pins 3, 4, 5, 7, 11, 13, 14)	−0.3	7.5	V
(pins 16, 19, 20, 21, 23, 24)	−0.3	7.5	V
(pins 8, 9)	−0.3	13.2	V

Temperatures

Storage temperature	T_{stg}	−20 to +125	°C
Operating ambient temperature	T_{amb}	−20 to +70	°C

CHARACTERISTICS

Supply voltage

	min.	typ.	max.	
V_{DD} (pin 12)	4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current

I_{DD}	–	20	50	mA

Inputs		min.	typ.	max.	
6 MHz - F6 (pin 2)					
Input voltage; HIGH	V_{IH}	3.5	–	6.5	V
Input voltage; LOW	V_{IL}	Note 1	–	0	V
Rise time (between 0 V and 3.5 V levels)		–	–	25	ns
Fall time (between 0 V and 3.5 V levels)		–	–	20	ns
Mark/space ratio (measured at 1.5 V level)		–	–	56:44	
All other inputs FLR (pin 6), FS (pin 10), $\overline{TLC}$ (pin 15), HIE (pin 16), $\overline{BCS}$ (pin 17, T/B (pin 18)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input leakage current (V_{in} = 5.5 V)		–	–	10	μA
Input capacitance		–	–	7	pF
Outputs					
TR6 (pin 3)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance		–	–	15	pF
Output rise time (Note 2)		–	–	30	ns
Output fall time (Note 2)		–	–	30	ns
Mark/space ratio		40:60	–	–	
F1 (pin 4)					
Output voltage; LOW (I_{OL} = 100 μA) Note 4	V_{OL}	0	–	0.4	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance		–	–	35	pF
Output rise time (Note 2)		–	–	50	ns
Output fall time (Note 2)		–	–	30	ns
Mark/space ratio		–	–	60:40	
Delay time (measured from rising edge of TR6) Note 3		7	–	60	ns
$\overline{AHS}$ (pin 5)					
Output voltage; LOW (I_{OL} = 100 μA) Note 5	V_{OL}	0	–	0.4	V
Output voltage; HIGH (I_{OH} = −200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		–	–	30	pF
Output rise time (Note 2)		–	–	100	ns
Output fall time (Note 2)		–	–	100	ns
Delay time (falling edge measured from F1 rising edge) Note 3		0	–	300	ns

CHARACTERISTICS (continued)

		min.	typ.	max.	
$\overline{GLR}$ (pin 7)					
Output voltage; LOW (I_{OL} = 0.9 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		–	–	40	pF
Output rise time } Note 2		–	–	60	ns
Output fall time } Note 2		–	–	50	ns
Delay time Note 3		0	–	200	ns
$\overline{PL}$ (pin 8) (Open drain)					
Output voltage; LOW (I_{OL} = 2 mA)	V_{OL}	0	–	1.0	V
Output current in off state (V_{OUT} = 6 V)		–	–	10	μA
Output load capacitance		–	–	30	pF
Output fall time Note 2		–	–	100	ns
Delay time Note 3		0	–	250	ns
$\overline{CBB}$ (pin 9) (Open drain)					
Output voltage; LOW (I_{OL} = 1 mA)	V_{OL}	0	–	1.0	V
Output current in off state (V_{OUT} = 6 V)		–	–	10	μA
Output load capacitance		–	–	30	pF
Output fall time Note 2		–	–	200	ns
Delay time Note 3		0	–	250	ns
CRS (pin 11)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		–	–	30	pF
Output rise time } Note 2		–	–	1	μs
Output fall time } Note 2		–	–	1	μs
LOSE (pin 13)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		–	–	30	pF
Output rise time } Note 2		–	–	50	ns
Output fall time } Note 2		–	–	50	ns
Delay time (measured from F1 falling edge) Note 3		0	–	250	ns
DEW (pin 14)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		–	–	42	pF
Output rise time } Note 2		–	–	200	ns
Output fall time } Note 2		–	–	200	ns
Delay time (measured from falling edge of $\overline{CBB}$) Note 3		7.5	–	8.5	μs

A_0, A_1, A_2 (pins 19, 20 and 21) 3-state

Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		–	–	85	pF
Output rise time } Note 2		–	–	1	μs
Output fall time } Note 2		–	–	1	μs
Delay time (measured from falling edge of $\overline{CBB}$) Note 3		−2	–	10	μs
Leakage current in 'off' state (V_{OUT} = 5.5 V)		–	–	10	μA
High impedance switching time					
Into high impedance state		0	–	0.9	μs
From high impedance state		1	–	2.9	μs

A_3, A_4 (pin 22 and 23) 3-state

Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V

All other parameters are as for A_0 to A_3

RACK (pin 24) 3-state

Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		–	–	40	pF
Output rise time } Note 2		–	–	60	ns
Output fall time } Note 2		–	–	300	ns
Delay time (measured from falling edge of F1) Note 3		150	–	280	ns
Leakage current in 'off' state (V_{OUT} = 5.5 V)		–	–	10	μA
High impedance switching time					
Into high impedance state		1	–	2.9	μs
From high impedance state		0	–	0.9	μs

Notes

1. This input incorporates an internal clamping diode.

The recommended input circuit is:

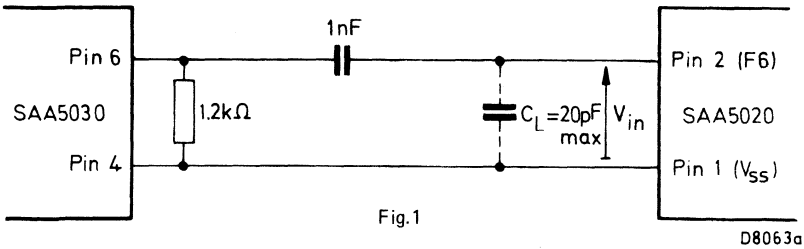


Fig.1

D8063a

2. Rise and fall times are measured between the 0.8 V and 2.0 V levels unless otherwise stated.
3. All delay times are measured from the rising edge of F1 unless otherwise stated.
   All delay times are measured at the 1.5 V level on the input to either the 2.0 V level on the rising edge of the output or the 0.8 V level on the falling edge of the output.

Notes (continued)

4. I_{OL} may be increased to 1 mA if load capacitance is less than 10 pF.
5. I_{OL} may be increased to 1.6 mA. Delay time will be increased to 350 ns max.

APPLICATION DATA

The function is quoted against the corresponding pin number.

For details of output waveforms see Fig.3

Pin No

1. V_{SS} Ground – 0 V
2. **F6**

   This input is the 6 MHz master clock signal and is used to derive the basic timings for the teletext display. It contains an internal diode clamp.
3. **TR6**

   This output is the 6 MHz character dot rate clock signal for the SAA5050 Teletext Character Generator.
4. **F1**

   This output is a 1 MHz character repetition rate clock signal for the SAA5040 Teletext Acquisition and Control device and the SAA5050 Teletext Character Generator.
   This output is synchronous with TR6, with a positive going edge occuring at time zero of the line.
5. **$\overline{\text{AHS}}$ After hours sync**

   This output signal is an internally generated TV compound sync signal which may be used to synchronise the display (Fig.2).
6. **FLR Fast line reset**

   This input from the SAA5030 Video Processor is used to reset the internal TV line rate counter. It is a positive going pulse of approximately 4.6 μs duration, and occurs during initial set-up of the phase locked system.
7. **$\overline{\text{GLR}}$ General line reset**

   This output is a TV line frequency signal used for reset and clock functions in the SAA5040 Teletext Acquisition and Control device, and the SAA5050 Teletext Character Generator. It is a 1 μs negative going pulse commencing 5 μs from the start of each line.
8. **$\overline{\text{PL}}$ Phase lock**

   This line frequency output signal to the SAA5030 Video Processor is used to phase lock the 6 MHz display system clock to the incoming television video signal. It is a 4 μs negative going pulse commencing at 62 μs into line
9. **$\overline{\text{CBB}}$ Colour burst blanking**

   This output signal is used to reset internal data processing and sync circuits within the SAA5030 Video Processor. It is an 8 μs negative going pulse starting at time zero of the line.
10. **FS Field sync**

    This input signal from the SAA5030 Video Processor is used to reset the field rate counter, to maintain correct field sync with incoming video.
11. **CRS Character rounding select**

    This output signal to the SAA5050 Teletext Character Generator is required for correct character rounding of small characters within the character generator. The output is high for even fields (0-313 lines) and low for odd fields (314-625 lines).

12. **V_{DD} + 5 V Supply**

This is the power supply input to the circuit.

13. **LOSE Load output shift register enable**

This output signal to the SAA5050 Teletext Character Generator is used to reset internal control character flip-flops prior to the start of each display line. This signal also defines the character display period. It is a positive going pulse of duration 40 μs starting 14.5 μs after the start of the line and occurs on lines 49 to 288 and 362 to 601 only.

14. **DEW Data entry window**

This output defines the period during which data may be extracted from the incoming television signal and written into the page memory. This signal is required by the SAA5040 Teletext Acquisition and Control device and the SAA5050 Teletext Character Generator. This is a positive going pulse commencing at the end of line 5 and finishing at end of line 22 and similarly for lines 318 and 335.

15. **$\overline{\text{TLC}}$ Transmitted large character**

This input from the SAA5050 Teletext Character Generator is to enable the correct display of large characters under broadcast control. It is high for normal character display and must be taken low for large character display.

16. **HIE High impedance enable**

This input when taken high will switch the address and address clock (RACK) outputs to their high impedance state. For normal teletext operation this input should be connected to the DEW output (Pin 14).

17. **$\overline{\text{BCS}}$ Big character select**

This input from the SAA5040 Teletext Acquisition and Control circuit is used to enable the correct display of large characters. It must be high for normal character display and taken low for large character display.

18. **$\overline{\text{T}}$/B Top or bottom select**

This input from the SAA5040 Teletext Acquisition and Control device controls the RAM row address logic for correct operation of page display when large character display has been selected under user control. It must be low for the top half to be displayed, and high for the bottom half.

19, 20, 21, 22, 23 **A_0 to A_4 Memory addresses**

These 3-state outputs to the teletext memory provide the RAM row addresses during the display period (i.e. TV lines 49 to 288 - 362 to 601 inclusive). These outputs switch to the high impedance state when HIE (pin 16) is taken high. All address outputs are low during line 40.

During display period the outputs provide a binary count sequence which is increased every ten lines in small character mode and every twenty lines in large character mode. If any row contains transmitted large characters the address is incremented by two after 20 lines.

24. **RACK Read address clock**

This 3-state output is a 1 MHz clock occuring during the display period of the line only. This output is used to clock the external RAM address counter during the display period. The output will switch to the high impedance state when HIE (pin 16) is taken high. The clock starts with a positive edge 14.65 μs from the start of a line and finishes with a negative going edge at 53.15 μs.

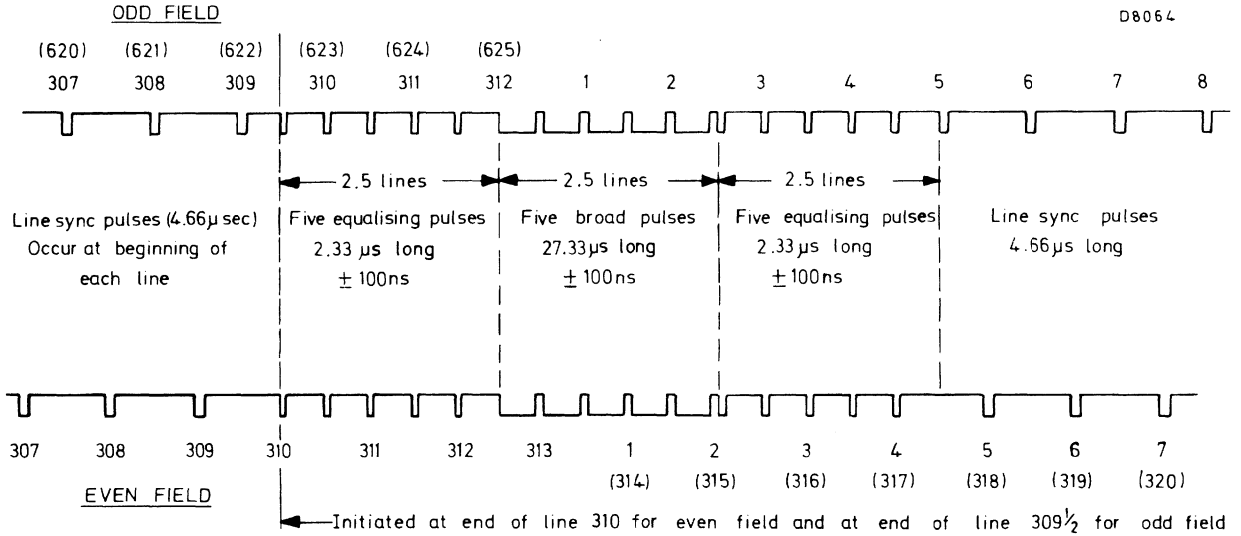


Fig. 2 After hours sync waveforms ($\overline{\text{AHS}}$)

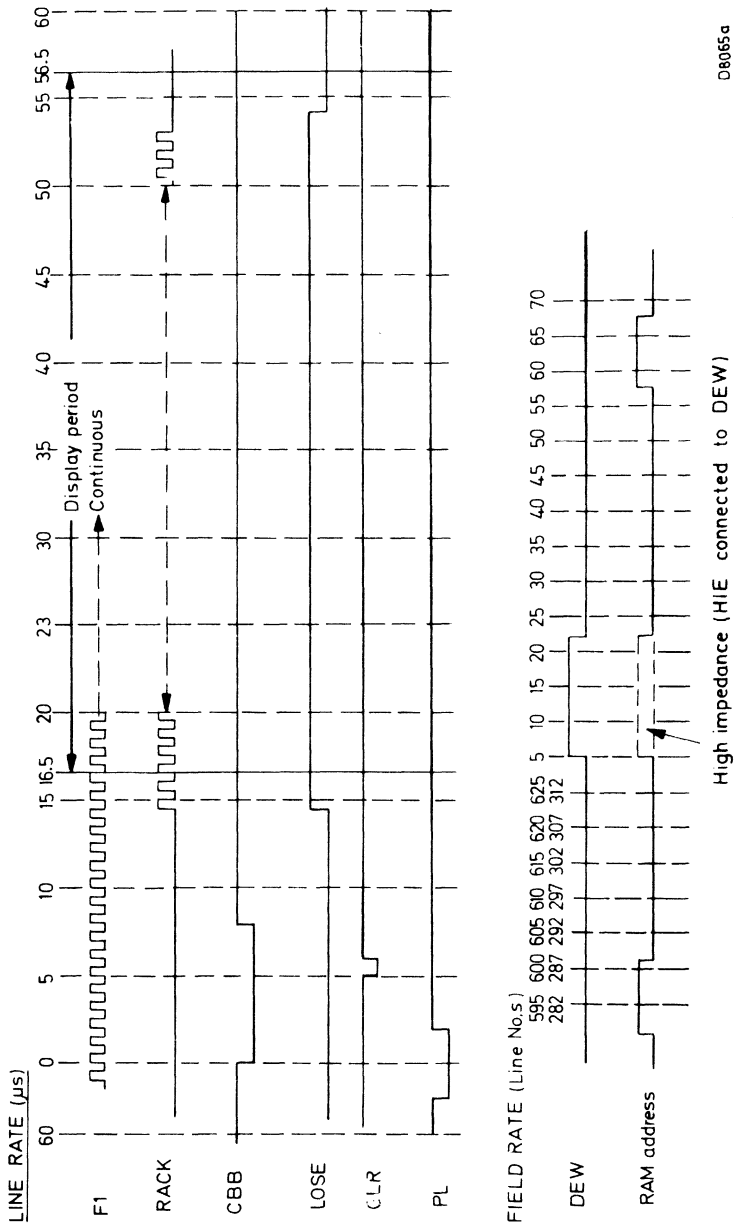


Fig.3 SAA5020 Output waveforms

TELETEXT VIDEO PROCESSOR

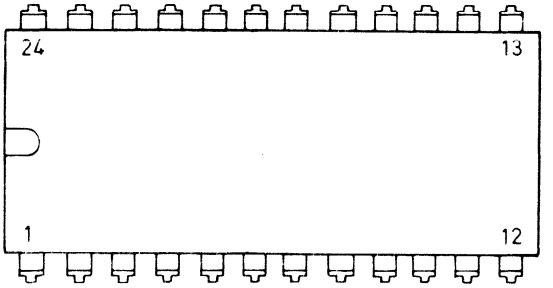
The SAA5030 is a monlithic bipolar integrated circuit used for teletext video processing. It is one of a package of four circuits to be used in teletext TV data systems. The SAA5030 extracts data and data clock information from the television composite video signal and feeds this to the Acquisition and Control circuit SAA5040. A 6 MHz crystal controlled phase locked oscillator is incorporated which drives the Timing Chain circuit SAA5020. An adaptive sync separator is also provided which derives line and field sync pulses from the input video in order to synchronise the timing chain.

QUICK REFERENCE DATA

Supply voltage	V_{supply}	nom	12	V
Supply current at V_{supply} = 12 V	I_{supply}	typ	110	mA
Video input amplitude (sync-white)	$V_{16\ video(p-p)}$	nom	2.4	V
Teletext data input amplitude	$V_{16\ teletext(p-p)}$	nom	1.1	V
Sync amplitude	$V_{16\ sync(p-p)}$	nom	0.7	V
Operating temperature range	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101 with heat spreader)



Viewed from top

PINNING

1. Signal presence time constant components.
2. Line reset time constant
3. Fast line reset output (FLR)
4. Ground (0V)
5. Sandcastle input ($\overline{PL}$ and $\overline{CBB}$)
6. 6 MHz output (F6)
7. Phase detector time constant components
8. 6 MHz crystal
9. 6 MHz crystal
10. Picture on input (PO)
11. After hours sync input ($\overline{AHS}$)
12. Sync output to TV
13. Field sync output (FS)
14. Field sync separator timing.
15. Sync separator capacitor
16. Composite video input
17. Supply voltage (+ve)
18. Clock output (F7)
19. $\overline{Data}$ output
20. Clock phase adjustment
21. Clock regenerator coil
22. Clock pulse timing capacitor
23. Peak detector capacitors
24. Peak detector capacitors

RATINGS Limiting values in accordance with the Absolute Maximum System.

Voltages					
Supply voltage	V_{17-4}	V_{supply}	max.	13.2	V
Input voltages	V_{5-4}	V_{in}	max.	9.0	V
	V_{10-4}	V_{in}	max.	V_{supply}	V
	V_{11-4}	V_{in}	max.	7.5	V
Dissipation				t.b.f.	W
Temperatures					
Storage temperature		T_{stg}		−20 to +125	°C
Operating ambient temperature		T_{amb}		−20 to +70	°C

CHARACTERISTICS (At T_{amb} = 25 °C, V_{supply} = 12 V and with external components as shown in Fig.1 unless otherwise stated)

			min.	typ.	max.	
Supply voltage	V_{17-4}	V_{supply}	10.8	12.0	13.2	V
Supply current (V_{supply} = 12.0 V)		I_{supply}	–	110	–	mA
Video input and sync separator						
Video input amplitude (sync to white) Fig.2		$V_{16\,video(p-p)}$	2.0	2.4	3.0	V
Source impedance, f = 100 kHz		Z_s	–	–	250	Ω
Sync amplitude		$V_{16\,sync(p-p)}$	0.07	0.7	1.0	V
Delay through sync separator			–	0.5	–	μs
Delay between field sync datum at pin 12 and the leading edge of separated field sync at pin 13 (Note 1, Fig.3)			32	48	62	μs
Field sync output						
V_{out} (low) at I_{13} = +20 μA		V_{13L}	–	–	0.5	V
V_{out} (high) at I_{13} = −100 μA		V_{13H}	2.4	–	–	V

Crystal controlled phase-locked oscillator

Measured using a crystal with the following specification e.g. catalogue no. 4322 143 03241

C_1 = 27.5 fF (typ)

C_0 = 6.8 pF (typ)

C_L = 20 pF

Trimability (C_L increased to 30 pF) > 750 Hz

Fundamental ESR < 50 Ω

		min.	typ.	max.	
Frequency	F6	–	6.0	–	MHz
Holding range		1.5	3.0	–	kHz
Catching range		1.5	3.0	–	kHz
Control sensitivity of phase detector measured as voltage at pin 7 with respect to phase difference between separated syncs and phase lock pulse $\overline{PL}$		–	0.3	–	mV/ns
Control sensitivity of oscillator measured as change in 6 MHz phase shift from pin 8 to pin 9 with respect to voltage at pin 7		–	2	–	deg/mV
Gain of sustaining amplifier, V_{9-8} measured with input voltage of 100 mV(p-p) and phase detector immobilised		2.5	–	–	V/V
Output voltage of 6 MHz signal at pin 6, measured into 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pin 6 into 20 pF load		–	–	30	ns

Data slicer and clock regenerator

Teletext data input amplitude, pin 16 (Note 2, Fig. 2); peak-to-peak value		–	1.1	–	V
Data input amplitude at pin 16 required to enable amplitude gate flip-flop (peak-to-peak value)		–	0.46	–	V
Attack rate, measured at pins 23 and 24 with a step to pin 16					
	Positive	–	15	–	V/μs
	Negative	–	9	–	V/μs
Decay rate, measured at pins 23 and 24 with a step input to pin 16		48	100	144	mV/μs
Width of clock coil drive pulses from pin 21 when clock amplitude is not being controlled (Note 3)		–	40	—	ns

Data slicer and clock regenerator (continued)	min.	typ.	max.	
Clock hangover measured at pin 18 as the time the clock coil continues ringing after the end of data (Note 4)	20	–		Clock Periods
Data and clock output voltages at pins 18 and 19 measured with 20 pF load capacitance; peak-to-peak value	–	5.5	–	V
Output rise and fall times at pins 18 and 19 into 20 pF loads	–	–	30	ns
Input voltage for energising clock phase setting circuit, pin 10	10	–	–	V
Sandcastle input				
Sandcastle detector thresholds, pin 5				
Phase lock pulse ($\overline{PL}$) on	2	–	–	V
Phase lock pulse off	–	–	3	V
Blanking pulse ($\overline{CBB}$) on	4.5	–	–	V
Blanking pulse off	–	–	5.5	V
Dual polarity sync buffer				
After hours sync ($\overline{AHS}$) pulse input pin 11				
Threshold for $\overline{AHS}$ active	1.0	–	–	V
Threshold for $\overline{AHS}$ off	–	–	2.0	V
Picture on (PO) input, pin 10				
Threshold for PO active	–	–	2.0	V
Threshold for PO off	1.0	–	–	V
Sync output, pin 12				
AHS output with pin 10 < 1 V (Note 5); peak-to-peak value	–	0.7	–	V
Composite sync output with pin 10 > 2 V (Notes 5 and 6); peak-to-peak value	–	0.7	1.0	V
Output current	–	–	3	mA
Line reset and signal presence detectors				
Schmitt trigger threshold on pin 2 to inhibit line reset output at pin 3 (syncs coincident)	–	6.2	–	V
Schmitt trigger threshold on pin 2 to permit line reset output at pin 3 (syncs non-coincident)	–	7.8	–	V
Line reset output V_{out} (low) at $I_3 = +20\ \mu A$	–	–	0.5	V
Line reset output V_{out} (high) at $I_3 = -100\ \mu A$	2.4	–	–	V
Signal presence Schmitt trigger threshold on pin 2 below which the circuit accepts the input signal	–	6.0	–	V
Signal presence Schmitt trigger threshold on pin 2 above which the input signal is rejected	–	6.3	–	V

Notes

1. This is measured with the dual polarity buffer external resistor connected to give negative going syncs. The measurement is made after adjustment of the potential divider at pin 14 for optimum delay.
2. The teletext data input contains binary elements as a two level NRZ signal shaped by a raised cosine filter. The bit rate is 6.9375 M bit/s. The use of odd parity for the 8 bit bytes ensures that there are never more than 14 bit periods between each data transition.
3. This is measured by replacing the clock coil with a small value resistor.
4. This must be measured with the clock coil tuned and using a clock-cracker signal into pin 16. The clock-cracker is a teletext waveform consisting of only one data transition in each byte.
5. With the external resistor connected to the ground rail, syncs are positive going centred on +2.3 V. With the resistor connected to the supply rail, syncs are negative going centred on +9.7 V.
6. When composite sync is being delivered, the level is substantially the same as that at the video input.

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. **Signal presence time constant**

   A capacitor and a resistor connected in parallel between this pin and supply determine the delay in operation of the signal presence detector.

2. **Line reset time constant**

   A capacitor between this pin and supply integrates current pulses from the coincidence detector; the resultant level is used to determine whether to allow FLR pulses (see pin 3).

3. **Fast line reset output (FLR)**

   Positive going sync pulses are produced at this output if the coincidence detector shows no coincidence between the syncs separated from the incoming video and the $\overline{CBB}$ waveform from the timing chain circuit SAA5020. These pulses are sent to the timing chain circuit and are used to reset its counters, so as to effect rapid lock-up of the phase locked loop.

4. **Ground** 0V

5. **Sandcastle input ($\overline{PL}$ and $\overline{CBB}$)**

   This input accepts a sandcastle waveform which is formed from $\overline{PL}$ and $\overline{CBB}$ from the timing chain SAA5020. PL is obtained by slicing the waveform at 2.5 V, and this, together with separated sync, are inputs to the phase detector which forms part of the phase locked loop. When the loop has locked up, the edges of PL are nominally 2 μs before and 2 μs after the leading edge of separated line syncs.
   CBB is obtained by slicing the waveform at 5 V, and is used to prevent the data slicer being offset by the colour burst.

6. **6 MHz output (F6)**

   This is the output of the crystal oscillator (see pins 8 and 9), and is taken to the timing chain circuit SAA5020 via a series capacitor.

7. **Phase detector time constant**

   The integrating components for the phase detector of the phase locked loop are connected between this pin and supply.

APPLICATION DATA *(continued)*

8,9 **6 MHz crystal**

A 6 MHz crystal in series with a trimmer capacitor is connected between these pins. It forms part of an oscillator whose frequency is controlled by the voltage on pin 7, which forms part of the phase locked loop.

10. **Picture on input (PO)**

The PO signal from the acquisition and control circuit SAA5040 is fed to this input and is used to determine whether the input video (pin 16) or the $\overline{\text{AHS}}$ waveform (pin 11) appears at pin 12.

11. **After hours sync ($\overline{\text{AHS}}$)**

A composite sync waveform $\overline{\text{AHS}}$ is generated in the timing chain circuit SAA5020 and is used to synchronise the TV (see pin 10).

12. **Sync output to TV**

Either the input video or $\overline{\text{AHS}}$ is available at this output dependent on whether the PO signal is high or low. In addition either signal may be positive-going or negative-going, dependent on whether the load resistor at this output is connected to ground or supply.

13. **Field sync output (FS)**

A pulse, derived from the input video by the field sync separator, which is used to reset the line counter in the timing chain circuit SAA5020.

14. **Field sync separator timing**

A capacitor and adjusting network is connected to this pin and forms the integrator of the field sync separator.

15. **Sync separator capacitor**

A capacitor connected to this pin forms part of the adaptive sync separator.

16. **Composite video input**

The composite video is fed to this input via a coupling capacitor.

17. **Supply voltage + 12 V**

18. **Clock output**

The regenerated clock, after extraction from the teletext data, is fed out to the acquisition and control circuit SAA5040 via a series capacitor.

19. **Data output**

The teletext data is sliced off the video waveform, squared up and latched within the SAA5030. The latched output is fed to the acquisition and control circuit SAA5040 via a series capacitor.

→ 20. **Clock decoupling**

A 1 nF capacitor between pin 20 and ground is required for clock decoupling.

21. **Clock regenerator coil**

A high-Q parallel tuned circuit is connected between this pin and an external potential divider. The coil is part of the clock regeneration circuit (see pin 22).

22. **Clock pulse timing capacitor**

Short pulses are derived from both edges of data with the aid of a capacitor connected to this pin. The resulting pulses are fed, as a current, into the clock coil connected to pin 21. Resulting oscillations are limited and taken to the acquisition and control circuit SAA5040 via pin 18.

23,24 **Peak detector capacitors**

The teletext data is sliced with an automatic data slicer whose slicing level is the mid-point of two peak detectors working on the video. Storage capacitors are connected to these pins for the negative and positive peak detectors.

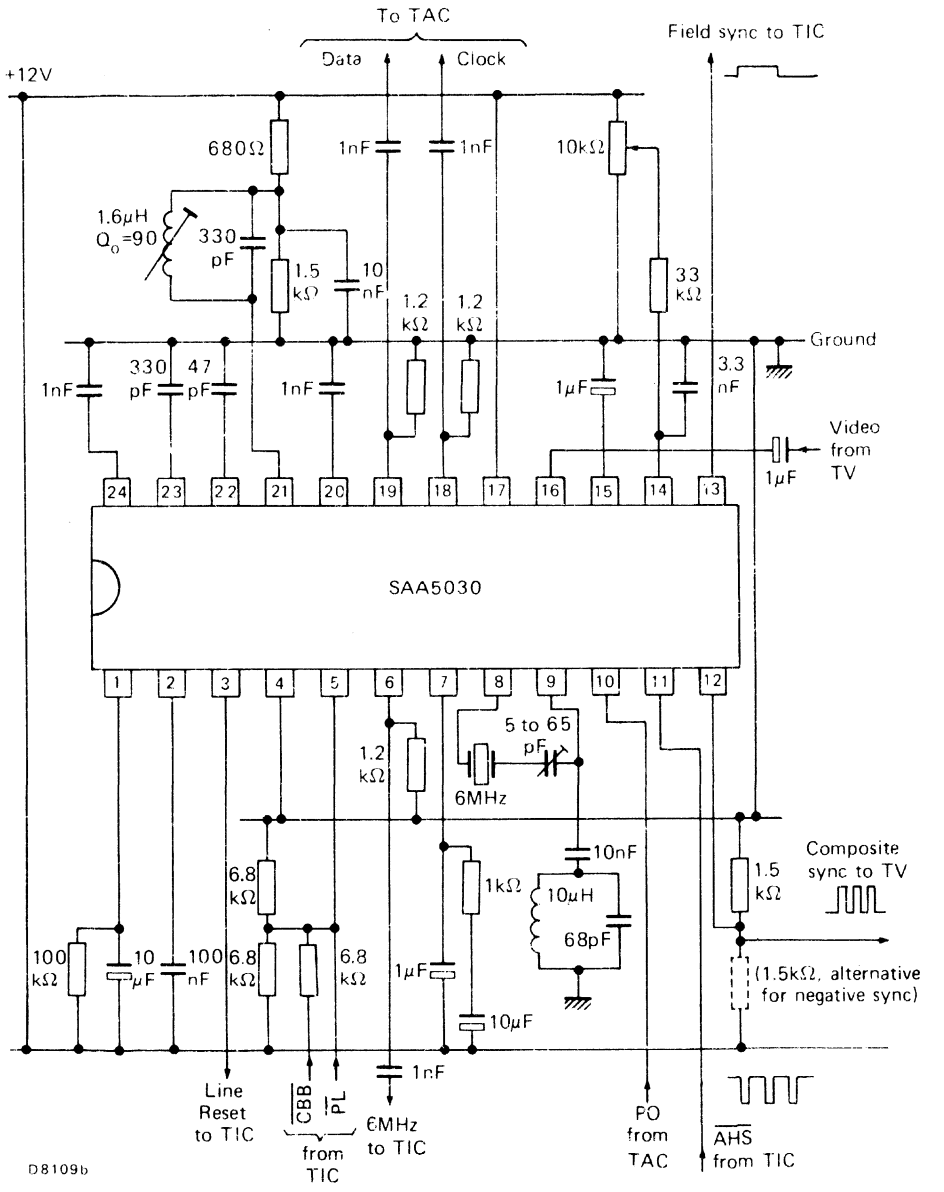


Fig.1 Peripheral circuit.

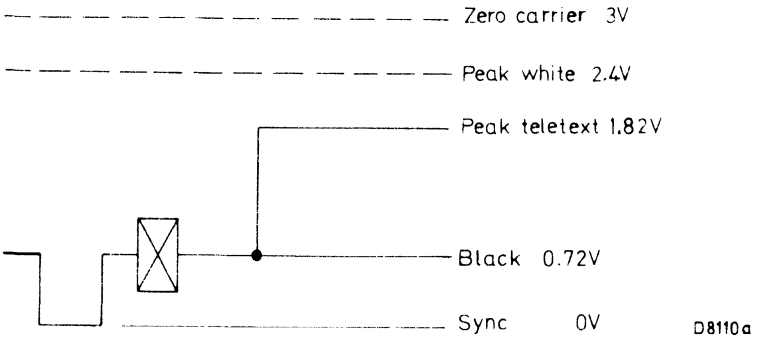


Fig. 2 Part of teletext line, with burst, showing nominal levels.

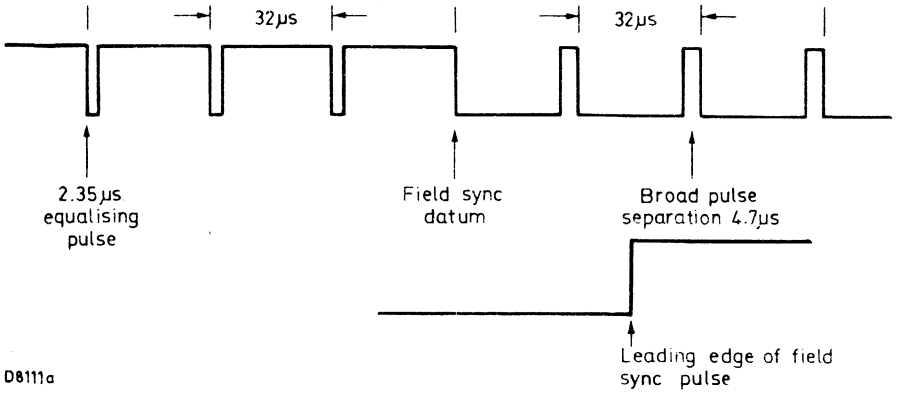


Fig. 3 Detail of idealised composite sync waveform.

TELETEXT ACQUISITION AND CONTROL CIRCUIT

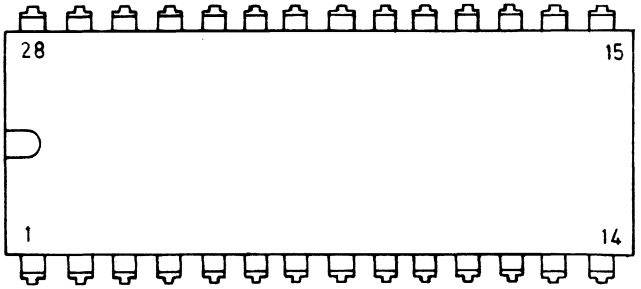
The SAA5040 is an MOS N-channel integrated circuit which performs the control, data acquisition and data routing functions of the teletext system.
The SAA5040 is a 28-lead device which receives serial teletext data from the SAA5030 video processor and data from the remote control system e.g. SAA5010. The SAA5040 selects the required page information and feeds it in parallel form to the teletext page memory.
The SAA5040 works in conjunction with the SAA5020 Timing Chain and the SAA5050 Character Generator.
The circuit is designed in accordance with the September 1976 Broadcast Teletext specification published by BBC/IBA/BREMA.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	80	mA
Operating ambient temperature	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117)



Viewed from top

Pinning: see next page

PINNING

1. V_{SS}
2. F7 Data } teletext from SAA5030
3. F7 Clock }
4. Not connected *
5. DLIM } Control from SAA5010
6. $\overline{DATA}$ }
7. Data entry window (DEW)
8. Picture on output (PO)
9. Display enable output (DE)
10. Big character select ($\overline{BCS}$)
11. Top/bottom ($\overline{T}$/B)
12. General line reset ($\overline{GLR}$)
13. 1 MHz Input (F1)
14. V_{DD}
15. Write O.K. ($\overline{WOK}$)
16. Data out to memory (D7)
17. Data out to memory (D6)
18. Data out to memory (D5)
19. Data out to memory (D4)
20. Data out to memory (D3)
21. Data out to memory (D2)
22. Data out to memory (D1)
23. Address out to memory (A_4)
24. Address out to memory (A_3)
25. Address out to memory (A_2)
26. Address out to memory (A_1)
27. Address out to memory (A_0)
28. Write address clock (WACK)

DESCRIPTION

The circuit consists of two main sections.

a) Data Acquisition

The basic input to this section is the serial teletext data stream (F7 Data) from the Video Processor Circuit SAA5030. This is clocked by a 6.9375 MHz clock also from the SAA5030. The incoming data stream is processed and sorted so that the page of data selected by the user is written as 7 bit parallel words into the system memory. Hamming and parity checks are performed on the incoming data to reduce errors. Provision is also made to process the control bits in the page header.

b) Control Section

The basic input to this section is the 7 bit serial data from the Remote Control Decoder SAA5010. This is clocked by the DLIM signal.
The remote control commands are decoded and the control functions are stored.
See Table 1 for full details of the remote control commands used in the SAA5040. The control section can also write data into the page memory independently of the data acquisition section. This gives an on screen display of certain user-selected functions, e.g. page number and programme name.
The data and address outputs to the system memory are set to high impedance state if certain remote control commands are received (e.g. viewdata mode). This is to allow another circuit to access the memory using the same address and data lines. The address lines are also high impedance while the SAA5040 is not writing into the memory.

* This pin must be connected to V_{SS} for ceramic packages.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see MOS Handling Notes).

RATINGS Limiting values in accordance with the Absolute Maximum System.

Voltages (with respect to pin 1)

		min.	max.	
Supply voltage (pin 14)	V_{DD}	−0.3	7.5	V
Input voltage All inputs		−0.3	7.5	V
Output voltage (pin 8)		−0.3	13.2	V
All other outputs		−0.3	7.5	V

Temperatures

Storage temperature	T_{stg}	−20 to +125	°C
Operating ambient temperature	T_{amb}	−20 to +70	°C

CHARACTERISTICS

		min.	typ.	max.	
Supply voltage					
V_{DD} (pin 14)		4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current					
I_{DD}		–	80	120	mA
Inputs					
F7 Data (pin 2), F7 Clock (pin 3)					
Input voltage; HIGH	V_{IH}	3.5	–	5.5	V
Input voltage; LOW Note 1	V_{IL}	–	–	0.5	V
Rise time } Note 2	t_r	–	–	30	ns
Fall time } Note 2	t_f	–	–	30	ns
Input resistance		–	5	–	MΩ
Input capacitance		–	–	7	pF

CHARACTERISTICS (continued)

		min.	typ.	max.	
F1 (pin 13)					
Input voltage; HIGH	V_{IH}	2.4	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Rise time (Note 3)	t_r	–	–	50	ns
Fall time (Note 3)	t_f	–	–	30	ns
Input capacitance		–	–	7	pF
Input leakage current (V_{in} = 0 to 5.5 V)		–	–	10	μA
All other inputs					
DLIM (pin 5), $\overline{DATA}$ (pin 6), DEW (pin 7), $\overline{GLR}$ (pin 12)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input capacitance		–	–	7	pF
Input leakage current (V_{in} = 0 to 5.5 V)		–	–	10	μA
Outputs					
DE (pin 9), $\overline{BCS}$ (pin 10), $\overline{T}$/**B** (pin 11) (With internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 200 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −50 μA for pin 9; I_{OH} = −30 μA for pin 10; I_{OH} = −20 μA for pin 11)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 40 pF)	t_r	–	–	10	μs
Output voltage fall time (C_L = 40 pF)	t_f	–	–	1	μs
Output capacitance		–	–	7	pF
Output current with output in HIGH state (V_{out} = 0.5 V)	I_{out}	−50	–	−500	μA
PO (pin 8) (With internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 140 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −50 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	10	μs
Output capacitance		–	–	7	pF
Output current with output in HIGH state (V_{out} = 0.5 V)	I_{out}	−50	–	−500	μA
D1 to D7 (pins 16 to 22) (3-state)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	100	ns
Leakage current in 'off' state (V_{out} = 0 to 5.5 V)		−10	–	10	μA
Output capacitance		–	–	7	pF

		min.	typ.	max.	
$\overline{\text{WOK}}$ (pin 15) (3-state with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 400 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time } (C_L = 80 pF) (Note 3)	t_r	–	–	50	ns
Output voltage fall time } (C_L = 80 pF) (Note 3)	t_f	–	–	100	ns
Output current with 3-state 'off' (V_{out} = 0.5 V)		−80	–	−500	μA
Output capacitance		–	–	7	pF
WACK (pin 28) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time } (C_L = 40 pF) (Note 3)	t_r	–	–	50	ns
Output voltage fall time } (C_L = 40 pF) (Note 3)	t_f	–	–	300	ns
Leakage current in 'off' state (V_{out} = 0 to 5.5 V)		−10	–	10	μA
Output capacitance		–	–	7	pF
A_0 to A_2 (pins 25 to 27 (3-state)					
Output voltage; LOW (I_{OL} = 200 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 90 pF) (Note 3)	t_r, t_f	–	–	300	ns
Leakage current in 'off' state (V_{out} = 0 to 5.5 V)		−10	–	10	μA
Output capacitance		–	–	7	pF
A_3 and A_4 (pins 23 and 24) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	300	ns
Leakage current in 'off' state (V_{out} = 0 to 5.5 V)		−10	–	10	μA
Output capacitance		–	–	7	pF

TIMING CHARACTERISTICS

Teletext Data and Clock (F7 Data + F7 Clock)

(Note 2 and figure 1)

F7 Clock cycle time	TT_{tc}	144	–	–	ns
F7 Clock duty cycle (HIGH to LOW)		30	–	70	%
F7 Clock to data set-up time	TT_{tds}	–	60	–	ns
F7 Clock to data hold time	TT_{tdh}	–	40	–	ns

TIMING CHARACTERISTICS (continued)

		min.	typ.	max.	
Control $\overline{DATA}$ and Clock ($\overline{DATA}$ + DLIM)					
(Note 3 and figure 2)					
DLIM cycle time	t_c	–	16	–	μs
DLIM duty cycle		–	50	–	%
DLIM to $\overline{DATA}$ set-up time	t_{ds}	–	14	–	μs
DLIM to $\overline{DATA}$ hold time	t_{dh}	–	14	–	μs
Writing Teletext data into Memory during DEW					
(Figure 3)					
WACK cycle time		1150	–	–	ns
WACK rising edge to $\overline{WOK}$ falling edge	t_{AWW}	250	–	450	ns
WACK rising edge to $\overline{WOK}$ rising edge	t_{WRW}	220	–	355	ns
$\overline{WOK}$ pulse width	t_{WFD}	300	–	–	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns
Row address set-up time before first $\overline{WOK}$	t_{RAW}	190	–	–	ns
Row address valid time after last $\overline{WOK}$	t_{RWR}	0	–	–	ns
Writing Header information into Memory during TV line 40					
(Figure 4)					
This arrangement is a combined phasing of the SAA5040 and the SAA5020 and is therefore referred to F1 input. The first $\overline{WOK}$ is related to F1 No. 14½ from the SAA5020.					
F1 Clock cycle time		1000	–	–	ns
Time from F1 to $\overline{WOK}$ falling edge	t_{wf}	300	–	500	ns
Time from F1 to $\overline{WOK}$ rising edge	t_{fw}	0	–	120	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns

Notes

1. These inputs may be a.c. coupled. Minimum rating is −0.3 V but the input may be taken more negative if a.c. coupled.
2. Transition times measured between 0.5 and 3.5 volt levels. Delay times are measured from 1.5 V level.
3. Transition times measured between 0.8 and 2.0 volt levels. Delay times are measured from 1.5 V level.

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. V_{SS} Ground - 0 V
2. **F7 Data**

   This input is a serial data stream of broadcast teletext data from the SAA5030 Video Processor, the data being at a rate of 6.9375 MHz.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
3. **F7 Clock**

   This input is a 6.9375 MHz clock from the SAA5030 Video Processor which is used to clock the teletext data acquisition circuitry. The positive edge of this clock is nominally at the centre of each teletext data bit.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
5. **DLIM Delimiter**

   This input from the SAA5010 Remote Control Receiver Decoder is used to clock remote control data into the SAA5040. The positive going edge of every second clock pulse is nominally in the centre of each remote control data bit.
6. **$\overline{\text{DATA}}$ Remote control data**

   This input is a 7 bit serial data stream from the SAA5010 Remote Control Receiver Decoder. This data contains the teletext and viewdata remote control user functions. The nominal data rate is 32 μs/bit. The remote control commands used in the SAA5040 are shown in Table 1.
7. **DEW Data entry window**

   This input from the SAA5020 Timing Chain defines the period during which received teletext data may be accepted by the SAA5040. This signal is also used to enable the 5 memory address outputs (pins 23 to 27) and the 7 bit parallel data output (pins 16 to 22).
8. **PO Picture on**

   This output to the SAA5010, SAA5030 and SAA5050 circuits is a static level used for the selection of TV picture video 'on' or 'off'. The output is HIGH for TV picture 'ON', LOW for TV picture 'OFF'. The output has an internal pull-up to V_{DD}.
9. **DE Display enable**

   This output to the SAA5050 Teletext Character Generator is used to enable the teletext display. The output is high for display enabled, low for display disabled.
   The output is also forced to the low state during the DEW and TV line 40 periods and when a teletext page is cleared.
   The output has an internal pull-up to V_{DD}.
10. **$\overline{\text{BCS}}$ Big Character select**

    This output to the SAA5020 Timing Chain and SAA5050 Character Generator is used to select double height character format under user control. The output is high for normal height characters, low for double height characters. It is also forced to the high state on page clear.
    The output has an internal pull-up to V_{DD}.
11. **$\overline{\text{T}}$/B Top/bottom**

    This output to the SAA5020 Timing Chain is used to select whether top or bottom half page is being viewed. The output is high for bottom half page and low for top half page. It is also forced to the low state on page clear.
    The output has an internal pull-up to V_{DD}.

APPLICATION DATA (continued)

12. **$\overline{\text{GLR}}$ General line reset**

This input from the SAA5020 Timing Chain is used as a reset signal for internal control and display counter.

13. **F1**

This input is a 1 MHz clock signal from the SAA5020 Timing Chain used to clock internal remote control processing and encoding circuits.

14. **V_{DD} +5 V Supply**

This is the power supply input to the circuit.

15. **$\overline{\text{WOK}}$ Write O.K.**

This 3-state output signal to the system memory is used to control the writing of valid data into the system memory. The signal is LOW to write, and is in the high impedance state when viewdata is selected. The three state buffer is enabled at the same time as the data outputs (see below). An internal pull-up device prevents the output from floating into the LOW state when the 3-state buffer is off.

16. 17, 18, 19, 20, 21, 22 **D7 to D1, Data outputs**

These 3-state outputs are the seven bit parallel data outputs to the system memory. The outputs are enabled at the following times:-

a) During the data entry window (DEW) to write teletext data into the memory. The data rate is 867 k bytes per second and is derived from the teletext data clock.

b) During TV line 40 for encoded status information about user commands (e.g. programme number), to be written into the memory. This period is known as EDIL (encoded data insertion line). The data rate is 1M byte per second and is derived from the 1 MHz display clock F1.

c) When the page is being cleared. In this case the data output is forced to the space code (0100000) during the display period for one field. This data is held at the space code from either TV line 40 (if page clear is caused by user command), or the received teletext data line causing the clear function, until the start of the data entry window (DEW) of the next field.

23, 24, 25, 26, 27 **A4 to A0 Memory addresses**

These 3-state outputs are the 5 bit row address to the page memory. This address specifies in which of 24 rows the teletext data is to be written. The outputs are enabled during the data entry period (DEW).

28. **WACK Write address clock**

This 3-state output is used to clock the memory address counter during the data entry period (DEW). The output is enabled only during this period. The positive-going edge of WACK is used to clock the address counter.

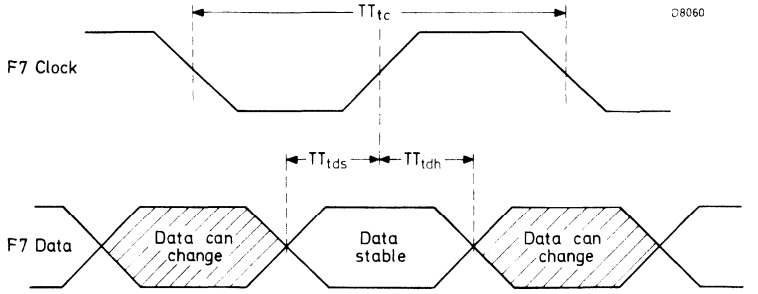


Fig. 1 Teletext data timing.

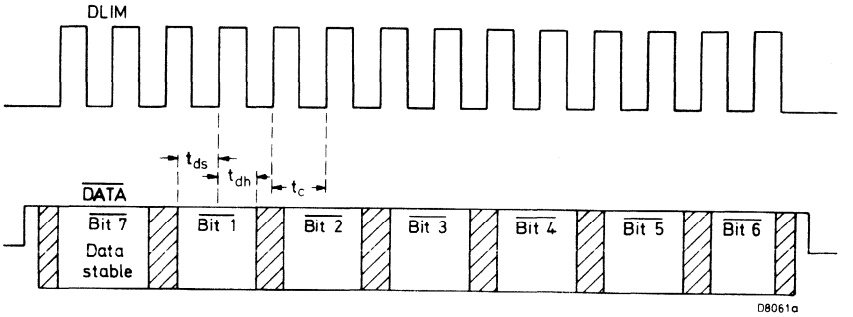


Fig. 2 Control clock and data timing.

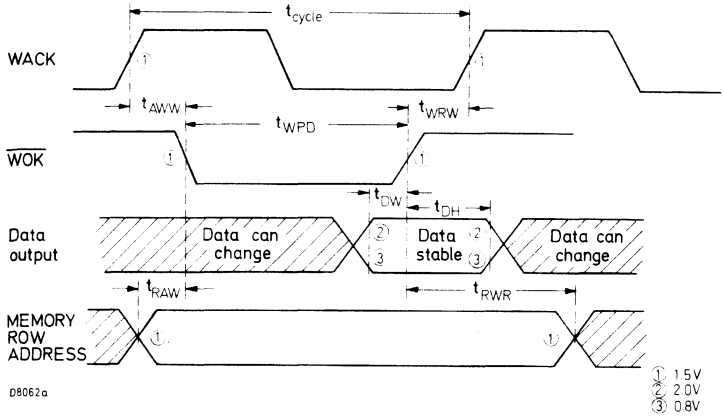


Fig. 3 Writing teletext data into memory during DEW.

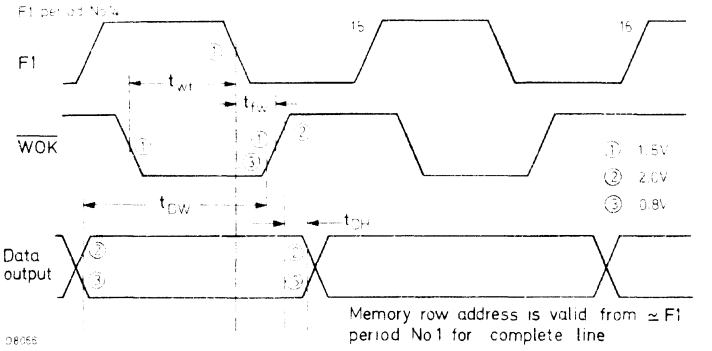


Fig. 4 Writing data into memory during TV line 40.

TABLE 1

Remote control commands used in the SAA5040

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$)	TELETEXT MODE ($b_7 = 1, b_6 = 0$)
0	0	0	0	0	RESET (Note 1)	
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1	TV/ON Gives programme display.	
0	0	1	0	0	STATUS Gives programme display.	STATUS Gives programme and header display.
0	0	1	0	1		HOLD Stops reception of teletext.
0	0	1	1	0		
0	0	1	1	1	TIME Gives time display.	DISPLAY CANCEL (Note 3)
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0		TAPE Resets to small characters.
0	1	1	0	1		
0	1	1	1	0		TIMED PAGE OFF
0	1	1	1	1		TIMED PAGE ON
1	0	0	0	0	PROGRAMMES (Note 2) BBC1	NUMBERS (Note 4) 1
1	0	0	0	1	PROGRAMMES (Note 2) ITV	NUMBERS (Note 4) 2
1	0	0	1	0	PROGRAMMES (Note 2) BBC2	NUMBERS (Note 4) 3
1	0	0	1	1	PROGRAMMES (Note 2) BBC1	NUMBERS (Note 4) 4
1	0	1	0	0	PROGRAMMES (Note 2) ITV	NUMBERS (Note 4) 5
1	0	1	0	1	PROGRAMMES (Note 2) VCR	NUMBERS (Note 4) 6
1	0	1	1	0	PROGRAMMES (Note 2) BBC1	NUMBERS (Note 4) 7
1	0	1	1	1	PROGRAMMES (Note 2) ITV	NUMBERS (Note 4) 8
1	1	0	0	0	PROGRAMMES (Note 2) BBC2	NUMBERS (Note 4) 9
1	1	0	0	1	PROGRAMMES (Note 2) BBC1	NUMBERS (Note 4) 0
1	1	0	1	0	PROGRAMMES (Note 2) ITV	SMALL CHARACTERS
1	1	0	1	1	PROGRAMMES (Note 2) VCR	LARGE CHARACTERS TOP HALF PAGE
1	1	1	0	0		LARGE CHARACTERS BOTTOM HALF PAGE
1	1	1	0	1		
1	1	1	1	0		SUPERIMPOSE
1	1	1	1	1		TELETEXT/ON (Note 5)

Notes on Page 12

Notes

1. Reset clears the page memory, sets page number to 100 and time code to 00.00, and resets timed page and display cancel modes.
2. Programme names are displayed for 5 seconds in a box at the top left of the screen in large characters. Programme commands clear the page memory except in timed page mode.
3. Display cancel removes the text and restores the television picture. The SAA5040 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required using the teletext/on command.
4. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.
5. The teletext/on command resets display cancel, hold and superimpose modes.
6. Status, timed page on, timed page off, numbers, superimpose and teletext/on commands all reset to top half page and produce a box round the header for five seconds. This allows the header to be seen even in the television picture is on (e.g. newsflash or display cancel modes).
7. In viewdata mode ($b_7 = b_6 = 1$) the SAA5040 is disabled and teletext cannot be received. All 3-state outputs are high impedance.
8. The table on Page 11 shows code required for functions specified. The SAA5010 transmits and the SAA5040 requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$. For full details of remote control data coding see SAA5010 data sheet.

TELETEXT ACQUISITION AND CONTROL CIRCUIT

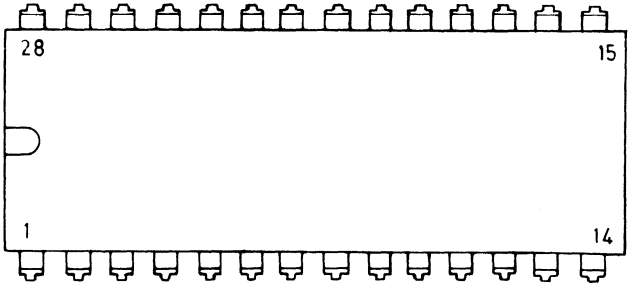
The SAA5041 is an MOS N-channel integrated circuit which performs the control, data acquisition and data routing functions of the teletext system.
The SAA5041 is a 28-lead device which receives serial teletext data from the SAA5030 video processor and data from the remote control system e.g. SAA5010. The SAA5041 selects the required page information and feeds it in parallel form to the teletext page memory.
The SAA5041 works in conjunction with the SAA5020 Timing Chain and the SAA5050 or SAA5052 Character Generator. It is similar to the SAA5040 but provides German on-screen displays and has a different set of remote control commands.
The circuit is designed in accordance with the September 1976 Broadcast Teletext specification published by BBC/IBA/BREMA.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	80	mA
Operating ambient temperature	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117)



Viewed from top

Pinning: see next page

PINNING

1. V_{SS}
2. F7 Data } teletext from SAA5030
3. F7 Clock }
4. Not connected *
5. DLIM } Control from remote control system
6. $\overline{DATA}$ }
7. Data entry window (DEW)
8. Picture on output (PO)
9. Display enable output (DE)
10. Big character select ($\overline{BCS}$)
11. Top/bottom ($\overline{T/B}$)
12. General line reset ($\overline{GLR}$)
13. 1 MHz Input (F1)
14. V_{DD}
15. Write O.K. ($\overline{WOK}$)
16. Data out to memory (D7)
17. Data out to memory (D6)
18. Data out to memory (D5)
19. Data out to memory (D4)
20. Data out to memory (D3)
21. Data out to memory (D2)
22. Data out to memory (D1)
23. Address out to memory (A_4)
24. Address out to memory (A_3)
25. Address out to memory (A_2)
26. Address out to memory (A_1)
27. Address out to memory (A_0)
28. Write address clock (WACK)

DESCRIPTION

The circuit consists of two main sections.

a) Data Acquisition

The basic input to this section is the serial teletext data stream (F7 Data) from the Video Processor Circuit SAA5030. This is clocked by a 6.9375 MHz clock also from the SAA5030. The incoming data stream is processed and sorted so that the page of data selected by the user is written as 7 bit parallel words into the system memory. Hamming and parity checks are performed on the incoming data to reduce errors. Provision is also made to process the control bits in the page header.

b) Control Section

The basic input to this section is the 7 bit serial data from the Remote Control Decoder (e.g. SAB3012 or SAA5010). This is clocked by the DLIM signal.
The remote control commands are decoded and the controlled functions are stored.
See Table 1 for full details of the remote control commands used in the SAA5041. The control section can also write data into the page memory independently of the data acquisition section. This gives an on screen display of certain user-selected functions, e.g. page number and programme name.
The data and address outputs to the system memory are set to high impedance state if certain remote control commands are received (e.g. Viewdata mode). This is to allow another circuit to access the memory using the same address and data lines. The address lines are also high impedance while the SAA5041 is not writing into the memory.

* This pin must be connected to V_{SS} for ceramic packages.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see MOS Handling Notes).

RATINGS Limiting values in accordance with the Absolute Maximum System.

Voltages (with respect to pin 1)

		min.	max.	
Supply voltage (pin 14)	V_{DD}	−0.3	7.5	V
Input voltage All inputs		−0.3	7.5	V
Output voltage (pin 8)		−0.3	13.2	V
All other outputs		−0.3	7.5	V

Temperatures

Storage temperature	T_{stg}	−20 to +125	°C
Operating ambient temperature	T_{amb}	−20 to +70	°C

CHARACTERISTICS

		min.	typ.	max.	
Supply voltage					
V_{DD} (pin 14)		4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current					
I_{DD}		–	80	120	mA
Inputs					
F7 Data (pin 2), F7 Clock (pin 3)					
Input voltage; HIGH	V_{IH}	3.5	–	5.5	V
Input voltage; LOW Note 1	V_{IL}	–	–	0.5	V
Rise time } Note 2	t_r	–	–	30	ns
Fall time } Note 2	t_f	–	–	30	ns
Input resistance		–	5	–	MΩ
Input capacitance		–	–	7	pF

CHARACTERISTICS (continued)

		min.	typ.	max.	
F1 (pin 13)					
Input voltage; HIGH	V_{IH}	2.4	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Rise time (Note 3)	t_r	–	–	50	ns
Fall time (Note 3)	t_f	–	–	30	ns
Input capacitance		–	–	7	pF
Input leakage current (V_{in} = 0 to 5.5 V)		–	–	10	μA
All other inputs					
DLIM (pin 5), $\overline{DATA}$ (pin 6), DEW (pin 7), $\overline{GLR}$ (pin 12)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input capacitance		–	–	7	pF
Input leakage current (V_{in} = 0 to 5.5 V)		–	–	10	μA
Outputs					
DE (pin 9), $\overline{\textbf{BCS}}$ (pin 10), $\overline{\textbf{T}}$/**B** (pin 11) (With internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 200 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −50 μA for pin 9; I_{OH} = −30 μA for pin 10; I_{OH} = −20 μA for pin 11)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 40 pF)	t_r	–	–	10	μs
Output voltage fall time (C_L = 40 pF)	t_f	–	–	1	μs
Output capacitance		–	–	7	pF
Output current with output in HIGH state (V_{out} = 0.5 V)	I_{out}	−50	–	−500	μA
PO (pin 8) (With internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 140 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −50 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	10	μs
Output capacitance		–	–	7	pF
Output current with output in HIGH state (V_{out} = 0.5 V)	I_{out}	−50	–	−500	μA
D1 to D7 (pins 16 to 22) (3-state)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	100	ns
Leakage current in 'off' state (V_{out} = 0 to 5.5 V)		−10	–	10	μA
Output capacitance		–	–	7	pF

		min.	typ.	max.	
WOK (pin 15) (3-state with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 400 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 80 pF) (Note 3)	t_r	–	–	50	ns
Output voltage fall time (C_L = 80 pF) (Note 3)	t_f	–	–	100	ns
Output current with 3-state 'off' (V_{out} = 0.5 V)		−80	–	−500	μA
Output capacitance		–	–	7	pF
WACK (pin 28) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 40 pF) (Note 1)	t_r	–	–	50	ns
Output voltage fall time (C_L = 40 pF) (Note 1)	t_f	–	–	300	ns
Leakage current in 'off' state (V_{out} = 0 to 5.5 V)		−10	–	10	μA
Output capacitance		–	–	7	pF
A_0 to A_2 (pins 25 to 27) (3-state)					
Output voltage; LOW (I_{OL} = 200 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 90 pF) (Note 3)	t_r, t_f	–	–	300	ns
Leakage current in 'off' state (V_{out} = 0 to 5,5 V)		−10	–	10	μA
Output capacitance		–	–	7	pF
A_3 and A_4 (pins 23 and 24) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	300	ns
Leakage current in 'off' state (V_{out} = 0 to 5.5 V)		−10	–	10	μA
Output capacitance		–	–	7	pF

TIMING CHARACTERISTICS

Teletext Data and Clock (F7 Data + F7 Clock)

(Note 2 and figure 1)

F7 Clock cycle time	TT_{tc}	144	–	–	ns
F7 Clock duty cycle (HIGH to LOW)		30	–	70	%
F7 Clock to data set-up time	TT_{tds}	–	60	–	ns
F7 Clock to data hold time	TT_{tdh}	–	40	–	ns

TIMING CHARACTERISTICS (continued)

		min.	typ.	max.	
Control $\overline{DATA}$ and Clock ($\overline{DATA}$ + DLIM)					
(Note 3 and figure 2)					
DLIM cycle time	t_c	–	16	–	µs
DLIM duty cycle		–	50	–	%
DLIM to $\overline{DATA}$ set-up time	t_{ds}	–	14	–	µs
DLIM to $\overline{DATA}$ hold time	t_{dh}	–	14	–	µs
Writing Teletext data into Memory during DEW					
(Figure 3)					
WACK cycle time		1150	–	–	ns
WACK rising edge to $\overline{WOK}$ falling edge	t_{AWW}	250	–	450	ns
WACK rising edge to $\overline{WOK}$ rising edge	t_{WRW}	220	–	355	ns
$\overline{WOK}$ pulse width	t_{WFD}	300	–	–	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns
Row address set-up time before first $\overline{WOK}$	t_{RAW}	190	–	–	ns
Row address valid time after last $\overline{WOK}$	t_{RWR}	0	–	–	ns
Writing Header information into Memory during TV line 40					
(Figure 4)					
This arrangement is a combined phasing of the SAA5041 and the SAA5020 and is therefore referred to F1 input. The first $\overline{WOK}$ is related to F1 No. 14½ from the SAA5020					
F1 Clock cycle time		1000	–	–	ns
Time from F1 to $\overline{WOK}$ falling edge	t_{wf}	300	–	500	ns
Time from F1 to $\overline{WOK}$ rising edge	t_{fw}	0	–	120	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns

Notes

1. These inputs may be a.c. coupled. Minimum rating is −0.3 V but the input may be taken more negative if a.c. coupled.
2. Transition times measured between 0.5 and 3.5 volt levels. Delay times are measured from 1.5 V level.
3. Transition times measured between 0.8 and 2.0 volt levels. Delay times are measured from 1.5 V level.

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. V_{SS} Ground - 0 V
2. **F7 Data**

   This input is a serial data stream of broadcast teletext data from the SAA5030 Video Processor, the data being at a rate of 6.9375 MHz.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
3. **F7 Clock**

   This input is a 6.9375 MHz clock from the SAA5030 Video Processor which is used to clock the teletext data acquisition circuitry. The positive edge of this clock is nominally at the centre of each teletext data bit.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
5. **DLIM Delimiter**

   This input from the remote control system (e.g. SAA5010) is used to clock remote control data into the SAA5041. The positive going edge of every second clock pulse is nominally in the centre of each remote control data bit.
6. **$\overline{\text{DATA}}$ Remote control data**

   This input is 7 bit serial data stream from the remote control system (e.g. SAA5010)
   This data contains the teletext and viewdata remote control user functions. The nominal data rate is 32 μs/bit. The remote control commands used in the SAA5041 are shown in Table 1.
7. **DEW Data entry window**

   This input from the SAA5020 Timing Chain defines the period during which received teletext data may be accepted by the SAA5041. This signal is also used to enable the 5 memory address outputs (pins 23 to 27) and the 7 bit parallel data output (pins 16 to 22).
8. **PO Picture on**

   This output to the SAA5010, SAA5030 and SAA5050 or SAA5052 circuits is a static level used for the selection of TV picture video 'on' or 'off'. The output is HIGH for TV picture ON, LOW for TV picture OFF. The output has internal pull-up to V_{DD}.
9. **DE Display enable**

   This output to the SAA5050 or SAA5052 Teletext Character Generators is used to enable the teletext display. The output is high for display enabled, low for display disabled.
   The output is also forced to the low state during the DEW and TV line 40 periods and when a teletext page is cleared.
   The output has an internal pull-up to V_{DD}.
10. **$\overline{\text{BCS}}$ Big Character select**

    This output to the SAA5020 Timing Chain and SAA5050 or SAA5052 Character Generators is used to select double height character format under user control. The output is high for normal height characters, low for double height characters. It is also forced to the high state on page clear.
    The output has an internal pull-up to V_{DD}.
11. **$\overline{\text{T}}$/B Top/bottom**

    This output to the SAA5020 Timing Chain is used to select whether top or bottom half page is being viewed. The output is high for bottom half page and low for top half page. It is also forced to the low state on page clear. The output has an internal pull-up to V_{DD}.

APPLICATION DATA (continued)

12. **$\overline{GLR}$ General line reset**

This input from the SAA5020 Timing Chain is used as a reset signal for internal control and display counter.

13. **F1**

This input is a 1 MHz clock signal from the SAA5020 Timing Chain used to clock internal remote control processing and encoding circuits.

14. **V_{DD} + 5 V Supply**

This is the power supply input to the circuit.

15. **$\overline{WOK}$ Write O.K.**

This 3-state output signal to the system memory is used to control the writing of valid data into the system memory. The signal is LOW to write, and is in the high impedance state when viewdata is selected. The three state buffer is enabled at the same time as the data outputs (see below). An internal pull-up device prevents the output from floating into the LOW state when the 3-state buffer is off.

16, 17, 18, 19, 20, 21, 22. **D7 to D1, Data outputs**

These 3-state outputs are the seven bit parallel data outputs to the system memory. The outputs are enabled at the following times:-

a) During the data entry window (DEW) to write teletext data into the memory. The data rate is 867 k bytes per second and is derived from the teletext data clock.

b) During TV line 40 for encoded status information about user commands (e.g. programme number), to be written into the memory. This period is known as EDIL (encoded data insertion line). The data rate is 1M byte per second and is derived from the 1 MHz display clock F1.

c) When the page is being cleared. In this case the data output is forced to the space code (0100000) during the display period for one field. This data is held at the space code from either TV line 40 (if page clear is caused by user command), or the received teletext data line causing the clear function, until the start of the data entry window (DEW) of the next field.

23, 24, 25, 26, 27. **A4 to A0 Memory addresses**

These 3-state outputs are the 5 bit row address to the page memory. This address specifies in which of 24 rows the teletext data is to be written. The outputs are enabled during the data entry period (DEW).

28. **WACK Write address clock**

This 3-state output is used to clock the memory address counter during the data entry period (DEW). The output is enabled only during this period. The positive-going edge of WACK is used to clock the address counter.

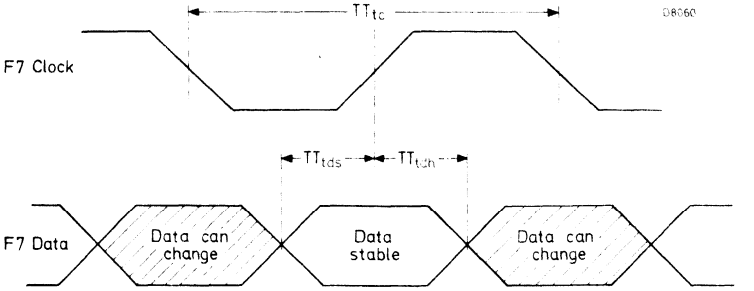


Fig. 1 Teletext data timing.

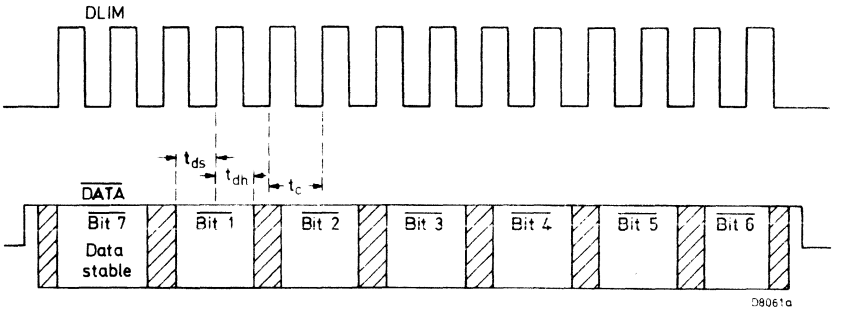


Fig. 2 Control clock and data timing.

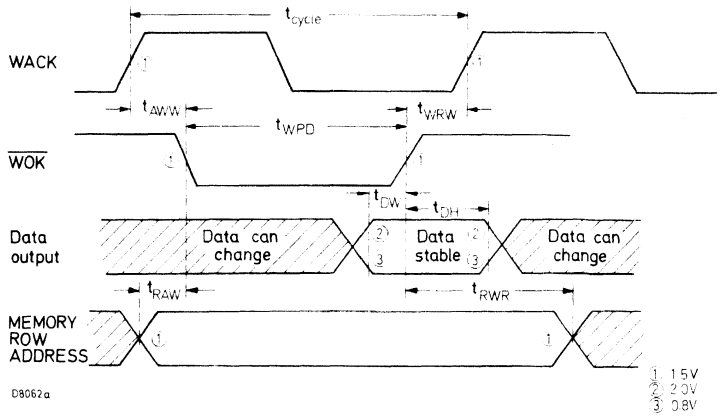


Fig. 3 Writing teletext data into memory during DEW.

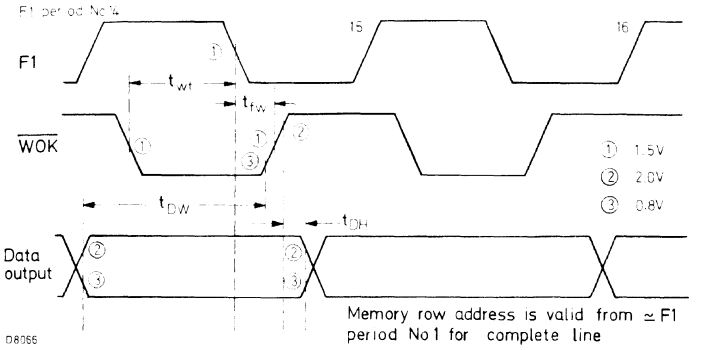


Fig. 4 Writing data into memory during TV line 40.

TABLE 1

Remote control command codes used in the SAA5041

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_6 = b_7 = 0$)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$)
0	0	0	0	0		
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1		
0	0	1	0	0	TIME Displays time.	STATUS Gives header and time display.
0	0	1	0	1		TIMED PAGE On/off toggle function.
0	0	1	1	0		
0	0	1	1	1		
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0		
0	1	1	0	1		
0	1	1	1	0		
0	1	1	1	1		TELETEXT RESET (Note 1)
1	0	0	0	0		0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1		5
1	0	1	1	0	PROGRAMMES Clear memory except	NUMBERS 6
1	0	1	1	1	in Timed Page mode	(Note 2) 7
1	1	0	0	0		8
1	1	0	0	1		9
1	1	0	1	0		SMALL CHARACTERS
1	1	0	1	1		LARGE CHARACTERS Top/bottom toggle function.
1	1	1	0	0		HOLD Stops reception of teletext (Note 3)
1	1	1	0	1		DISPLAY CANCEL (Note 4)
1	1	1	1	0		SUPERIMPOSE
1	1	1	1	1		NORMAL DISPLAY (Note 5)

Notes on page 12

Notes

1. The teletext reset command clears the page memory, selects page 100, goes to small characters and resets hold, timed page and display cancel modes.
2. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page is requested the header turns green and the page numbers roll until a new page is captured.
3. When hold mode is selected HALT is displayed in green at the top right of the screen.
4. Display cancel removes the text and restores the television picture. The SAA5041 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required using the normal display command.
5. The normal display command resets hold, display cancel and superimpose modes.
6. Status, timed page, numbers, hold, superimpose and normal display commands all reset to top half page and produce a box around the header for five seconds. This allows the header to be seen even if the television picture is on (e.g. newsflash or display cancel modes).
7. An S is displayed before the page number at the top left of the screen (e.g. S123).
8. In viewdata mode ($b_7 = b_6 = 1$) the SAA5041 is disabled and teletext cannot be received. All 3-state outputs are high impedance.
9. The table on Page 11 shows code required for functions specified. The SAA5041 requires the inverse of these codes i.e. $\overline{b}_7$ to $\overline{b}_1$. The code is received serially in the following order: $\overline{b}_7, \overline{b}_1, \overline{b}_2, \overline{b}_3, \overline{b}_4, \overline{b}_5, \overline{b}_6$.

TELETEXT CHARACTER GENERATOR

(ENGLISH)

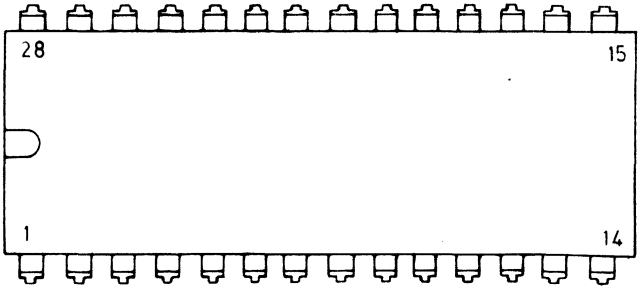
The SAA5050 is an MOS N-channel integrated circuit which provides the video drive signals to the television necessary to produce the teletext/viewdata display.
The SAA5050 is a 28 pin device which incorporates a fast access character generator ROM (4.3 k bits), the logic decoding for all the teletext control characters and decoding for some of the remote control functions.
The circuit generates 96 alphanumeric and 64 graphic characters. In addition there are 32 control characters which determine the nature of the display.
The SAA5050 is suitable for direct connection to the SAA5010, SAA5020 and SAA5040 integrated circuits.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom	5	V
Supply current	I_{DD}	typ.	85	mA
Operating ambient temperature	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117)



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Pinning: see next page

PINNING

1. V_{SS}
2. Superimpose
3. Remote control data ($\overline{DATA}$)
4. Character data input 1 (D1)
5. Character data input 2 (D2)
6. Character data input 3 (D3)
7. Character data input 4 (D4)
8. Character data input 5 (D5)
9. Character data input 6 (D6)
10. Character data input 7 (D7)
11. Remote control data clock (DLIM)
12. General line reset ($\overline{GLR}$)
13. Data entry window (DEW)
14. Character rounding select (CRS)
15. Big character select ($\overline{BCS}$)
16. Transmitted large character ($\overline{TLC}$)
17. Not connected
18. V_{DD}
19. 6 MHz Input (TR6)
20. 1 MHz Input (F1)
21. Monochrome video output (Y)
22. Blue output (B)
23. Green output (G)
24. Red output (R)
25. Blanking output
26. Load output shift register enable (LOSE)
27. Picture on input (PO)
28. Display enable input (DE)

DESCRIPTION

The basic input to the SAA5050 is the character data from the teletext page memory. This is a 7 bit code. Each character code defines a dot matrix pattern. The character period is 1 μs and the character dot rate is 6 MHz. The timings are derived from the two external input clocks F1 (1 MHz) and TR6 (6 MHz) which are amplified and re-synchronised internally. Each character rectangle is 6 dots wide by 10 TV lines high. One dot space is left between adjacent characters, and there is one line space left between rows. Alphanumeric characters are generated on a 5 x 9 matrix, allowing space for descending characters. Each of the 64 graphics characters is decoded to form a 2 x 3 block arrangement which occupies the complete 6 x 10 dot matrix (Fig.3). Graphics characters may be either contiguous or separated (Fig.4). The alphanumeric characters are character rounded, i.e. a half dot is inserted before or after a whole dot in the presence of a diagonal in a character matrix.

The character video output signals comprise a monochrome signal and RGB signals for a colour receiver. A blanking output signal is provided to blank out the television video signal when a newsflash or subtitle is to be displayed.

The monochrome data signal can be used to inlay characters into the television video. The use of the 32 control characters provides information on the nature of the display, e.g. colour. These are also used to provide other facilities such as 'concealed display' and flashing words etc. The full character set is given in Table 1.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (See MOS Handling Notes).

RATINGS Limiting values in accordance with the Absolute Maximum System.

		min.	typ.	max.	
Voltages (with respect to pin 1)					
Supply voltage (pin 18)		−0.3	–	7.5	V
Input voltages	All inputs + input/output	−0.3	–	7.5	V
Output voltage (pin 16)		−0.3	–	7.5	V
	All other outputs	−0.3	–	14.0	V
Temperature					
Storage temperature	T_{stg}		−20 to +125		°C
Operating ambient temperature	T_{amb}		−20 to +70		°C

CHARACTERISTICS

Supply voltage		min.	typ.	max.	
V_{DD} (pin 18)		4.5	–	5.5	V

The following parameters apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current					
I_{DD}		–	85	160	mA
Inputs					
Character data D1 to D7 (pins 4–10)					
Input voltage; HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Data set-up time (see Fig.2)		150	–	–	ns
Data hold time (see Fig.2)		100	–	–	ns
Clock inputs F1 (pin 20) **TR6** (pin 19)					
Input voltage; HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Logic inputs					
$\overline{DATA}$ (pin 3) DEW (pin 13) LOSE (pin 26) DLIM (pin 11) $\overline{CRS}$ (pin 14) PO (pin 27) $\overline{GLR}$ (pin 12) $\overline{BCS}$ (pin 15) DE (pin 28)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
All inputs					
Input leakage (V_{in} 5.5 V)		–	–	10	μA
Input capacitance		–	–	7	pF

CHARACTERISTICS (continued)

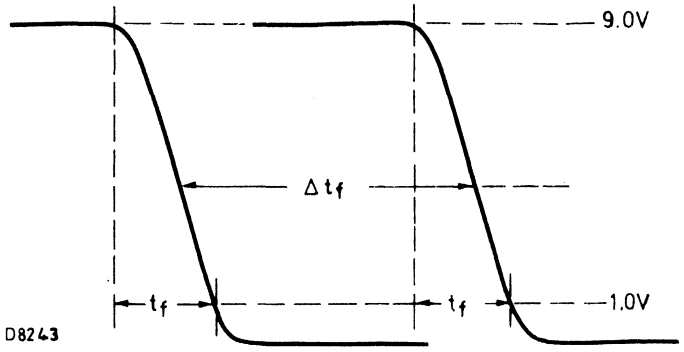
		min.	typ.	max.	
Outputs					
Character video outputs + Blanking output (Open drain)					
B - (pin 22), G - (pin 23), R - (pin 24), Y - (pin 21), Blanking (pin 25)					
Output voltage; LOW (I_{OL} = 2 mA)	V_{OL}	–	–	0.5	V
Output voltage; LOW (I_{OL} = 4 mA)		–	–	1.0	V
Output voltage; LOW (I_{OL} = 6 mA)		–	–	2.0	V
Output voltage; HIGH	V_{OH}	V_{DD}	–	13.2	V
Output load capacitance		–	–	15	pF
Output fall time t_f (Note 1)		–	–	30	ns
Variation of fall time between any outputs Δt_f (Note 1)		0	–	20	ns
$\overline{\text{TLC}}$ (pin 16)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		–	–	30	pF
Output rise time (Measured between 0.8 V and 2.0 V levels)		–	–	1.0	μs
Output fall time (Measured between 0.8 V and 2.0 V levels)		–	–	1.0	μs
Input/output					
$\overline{\text{Superimpose}}$ (pin 2) (Open drain)					
Input voltage; HIGH	V_{IH}	2.0	–	6.5	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input leakage (V_{in} = 5.5 V)		–	–	10	μA
Input capacitance		–	–	7	pF
Output voltage; LOW (I_{OL} = 0.4 mA)	V_{OL}	0	–	0.5	V
Output voltage; LOW (I_{OL} = 1.3 mA)	V_{OL}	0	–	1.0	V
Output load capacitance		–	–	45	pF
Output voltage; HIGH state (Note 2)	V_{OH}	–	–	6.5	V

Notes

1. Fall time, t_f and Δt_f, are defined as shown and are measured using the circuit shown below:

   t_f is measured between the 9 V and 1 V levels.

   Δt_f is the maximum time difference between outputs.



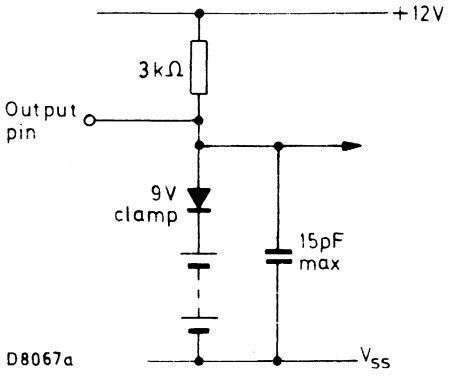


Fig.1

2. Recommended pull-up resistor for $\overline{\text{Superimpose}}$ is 18 kΩ.
3. The R,G,B,Y and blanking outputs are protected against short circuit to supply rails.

SPECIAL FEATURES

Flash oscillator

The circuit generates a 0.75 Hz signal with a 3:1 ON/OFF ratio to provide the flashing character facility.

Power-on-reset

When the supply voltage is switched on, the character generator will reset to TV, conceal and not superimpose modes.

SPECIAL FEATURES (continued)

Character rounding

The character rounding function is different for the small and double height characters. In both cases the ROM is accessed twice during the character period of 1 μs. The dot information of two rows is then compared to detect the presence of any diagonal in the character matrix and to determine the positioning of the character rounding half dots.
For small characters rounding is always referenced in the same direction (i.e. row before in even fields and row after in odd fields as determined by the CRS signal).
For double height characters rounding is always referenced alternately up and down changing every line using an internally generated signal. (The CRS signal is '0' for the odd field and '1' for the even field of an interlaced TV picture.)

Graphics decoder

The 64 graphics characters are decoded directly from the character data inputs and they appear on a 2 x 3 matrix. Figure 3 gives details of the graphics decoding.

APPLICATION DATA

The function is quoted against the corresponding pin numbers

Pin No.

1. V_{SS} Ground - 0 V

2. **$\overline{\text{Superimpose}}$**

   This is a dual purpose input/output pin. The output is an open drain transistor (capable of sinking current to V_{SS}), which is in the conducting state when superimpose mode is selected. This allows contrast reduction of the TV picture in superimpose mode if required. If the pin is held low, the internal 'TV mode' flip-flop is held in the 'text' state. This is for VDU applications when the remote control is not used.

3. **$\overline{\text{DATA}}$ Remote control data**

   This input accepts a 7-bit serial data stream from the SAA5010 remote control receiver decoder. This data contains the teletext and viewdata remote control user functions. The command codes used in the SAA5050 are shown in Table 2.

4, 5, 6, 7, 8, 9, 10. **Character data D1 to D7**

   These inputs accept a 7-bit parallel data code from the page memory. This data selects the alphanumeric characters, the graphics characters and the control characters. The alphanumeric addresses are ROM column addresses, the graphics and control data are decoded internally.

11. **DLIM**

    This input receives a clock signal from the SAA5010 remote control receiver decoder. This signal is used to clock remote control data from the SAA5010 into the remote control data input (Pin 3).

12. **$\overline{\text{GLR}}$ General line reset**

    This input signal from the SAA5020 Timing Chain is required for internal synchronisation of remote control data signals.

13. **DEW Data entry window**

    This input signal from the SAA5020 Timing Chain is required to reset the internal ROM row address counter prior to the display period. It is also used internally to derive the 'flash' period.

14, **CRS Character rounding select**

This input signal from the SAA5020 Timing Chain is required for correct character rounding of displayed characters. (Normal height characters only).

15. **$\overline{\text{BCS}}$ Big character select**

This input from the SAA5040 Teletext Acquisition and Control device allows selection of large characters by remote control.

16. **$\overline{\text{TLC}}$ Transmitted large characters**

This output to the SAA5020 Timing Chain enables double height characters to be displayed as a result of control characters stored in the page memory.

18. **V_{DD} + 5 V supply**

This is the power supply input to the circuit.

19. **TR6**

This input is a 6 MHz signal from the SAA5020 Timing Chain used as a character dot rate clock.

20. **F1**

This input is a 1 MHz equal mark/space ratio signal from the SAA5020 Timing Chain. It is used to latch the 7-bit parallel character data into the input latches. It is also used to synchronise an internal divide-by 6 counter. The F1 signal is internally synchronised with TR6.

21. **Y Output (Monochrome)**

This is a video output signal which is active in the high state containing character dot information for TV display.
The output is an open drain transistor capable of sinking current to V_{SS}.

22, 23, 24. **Blue, Green, Red outputs**

These are the Blue, Green and Red Character video outputs to the TV display circuits. They are active high and contain both character and background colour information.
The outputs are open drain transistors capable of sinking current to V_{SS}.

25. **Blanking**

This active high output signal provides TV picture video blanking. It is active for the duration of a box when Picture on and Display enable are high. It is also activated permanently for normal teletext display when no TV picture is required (PO low). The output is an open drain transistor capable of sinking current to V_{SS}. Full details given in Table 3.

26. **LOSE Load output shift register enable**

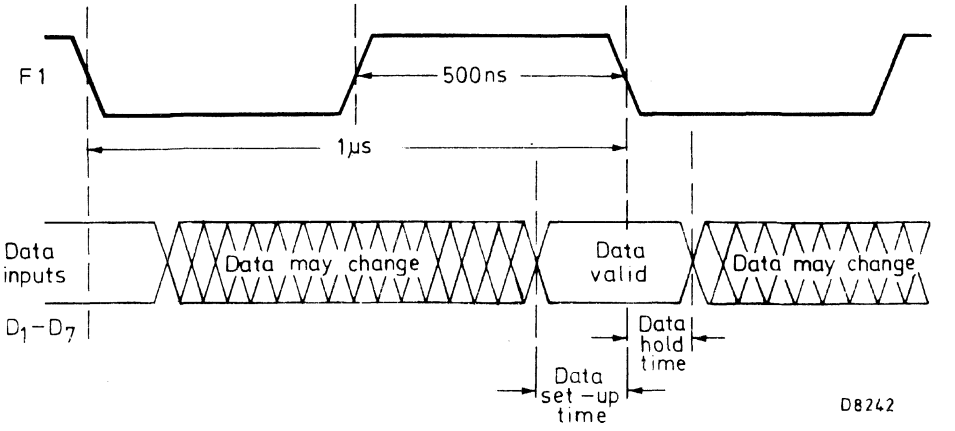
This input signal from the SAA5020 Timing Chain resets the internal control character flip-flops prior to the start of each display line.
This signal also defines the character display period.

27. **PO Picture on**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to control the character video and blanking outputs. When PO is high, only text in boxes is displayed unless in superimpose mode. The input is high for TV picture video on, low for picture off. See Table 3.

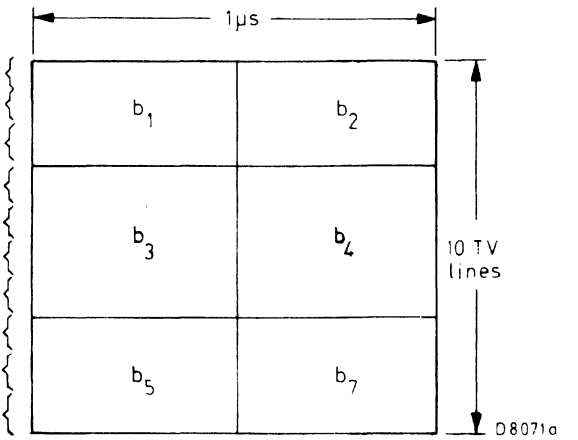
28. **DE Display enable**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to enable the teletext display. The input is high for teletext display enabled, low for display cancelled. See Table 3.



Note: All timings measured at 1.5 V level.

Fig. 2 Data input timing.



Each cell is illuminated if particular 'bit' (b_1, b_2, b_3, b_4, b_5, or b_7) is a '1'.
For graphics characters b_6 is always a 1 - See Table 1

Fig. 3 Graphics Character.

SAA5050 CHARACTER SET

D8068a

Bits b_4 b_3 b_2 b_1	Row	Col 0	Col 1	Col 2	Col 2a	Col 3	Col 3a	Col 4	Col 5	Col 6	Col 6a	Col 7	Col 7a
0 0 0 0	0	NUL *	DLE *			0		@	P	–		p	
0 0 0 1	1	Alpha Red	Graphics Red	!		1		A	Q	a		q	
0 0 1 0	2	Alpha Green	Graphics Green	"		2		B	R	b		r	
0 0 1 1	3	Alpha Yellow	Graphics Yellow	£		3		C	S	c		s	
0 1 0 0	4	Alpha Blue	Graphics Blue	$		4		D	T	d		t	
0 1 0 1	5	Alpha Magenta	Graphics Magenta	%		5		E	U	e		u	
0 1 1 0	6	Alpha Cyan	Graphics Cyan	&		6		F	V	f		v	
0 1 1 1	7	Alpha White **	Graphics White	'		7		G	W	g		w	
1 0 0 0	8	Flash	Conceal Display	(		8		H	X	h		x	
1 0 0 1	9	Steady **	Contiguous Graphics **	)		9		I	Y	i		y	
1 0 1 0	10	End Box **	Separated Graphics	*		:		J	Z	j		z	
1 0 1 1	11	Start Box **	ESC *	+		;		K	←	k		¼	
1 1 0 0	12	Normal Height **	Black Background **	,		<		L	½	l		‖	
1 1 0 1	13	Double Height	New Background	–		=		M	→	m		¾	
1 1 1 0	14	SO *	Hold Graphics	.		>		N	↑	n		÷	
1 1 1 1	15	SI *	Release Graphics **	/		?		O	#	o		■	

Control characters shown in columns 0 and 1 are normally displayed as spaces.

* These control characters are reserved for compatability with other data codes.

** These control characters are presumed before each row begins.

Codes may be referred to by their column and row e.g. 2/5 refers to %

Character rectangle

Black represents display colour.

White represents background.

Table 1

TABLE 2

Remote control command codes used in the SAA5050

CODE b_7	b_6	b_5	b_4	b_3	b_2	b_1	COMMAND	FUNCTION
0	X	X	X	X	X	X	'TV' mode	Allows text on top row of display only.
1	X	X	X	X	X	X	'Text' mode	Allows text throughout display period.
1	0	1	1	1	1	0	Superimpose	Sets superimpose mode.
1	0	1	1	1	1	1	Teletext	Resets superimpose mode.
0	X	X	X	X	X	X	'TV' mode	Resets superimpose mode.
1	1	X	X	X	X	X	Viewdata mode.	Resets superimpose mode.
1	X	0	0	1	1	0	Reveal	Reveals for time-out (notes 3, 4).
1	X	0	1	0	1	1	Reveal set	Sets reveal mode (note 3).
Any command apart from reveal set.								Resets reveal mode (note 3).

X = Don't care.

Notes

1. When the power is applied the SAA5050 is set into the 'TV' mode and reset out of superimpose and reveal modes.
2. 'Text' mode is selected when the $\overline{\text{superimpose}}$ pin is held low.
3. Reveal mode allows display of text previously concealed by 'conceal display' control characters.
4. This code is sent from the SAA5010 as a repeated command. Thus reveal mode is set for as long as the reveal key is depressed. The SAA5050 reverts to normal 'not reveal' mode 160 ms after the last reveal command.
5. The superimpose output is low only if superimpose mode is set and the DE (display enable) input is high.
6. The above table shows code required for functions specified.
   The SAA5010 transmits and the SAA5050 requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$ $\overline{b_1}$ $\overline{b_2}$ $\overline{b_3}$ $\overline{b_4}$ $\overline{b_5}$ $\overline{b_6}$. For full details of remote control data coding see SAA5010 data sheet.

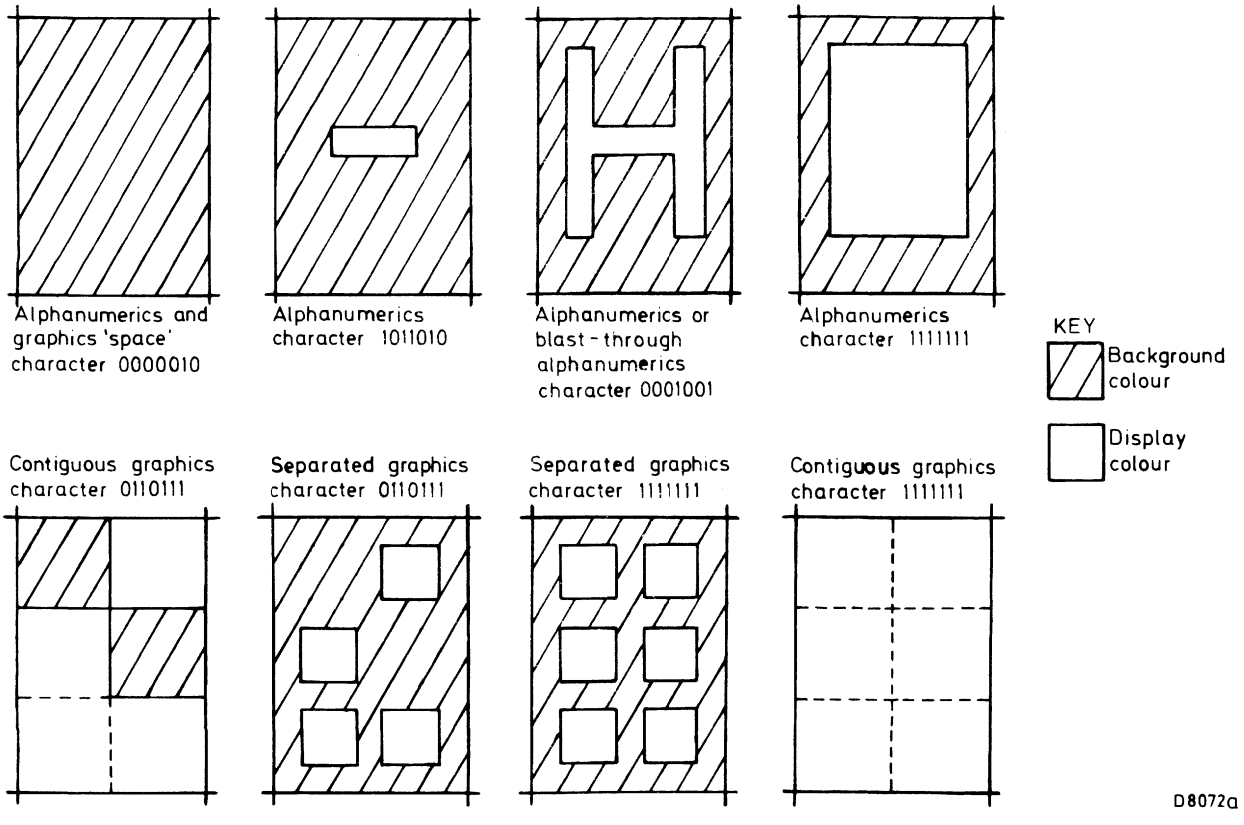
TABLE 3

Conditions affecting display

	Inputs		Control data		Outputs	
	Picture On (PO)	Display Enable (DE)	Superimpose Mode	Box	Text Display Enabled (i.e. R, G, B, Y outputs)	Blanking
(a)	1	0	1 or 0	1 or 0	0	0
(b)	0	1	1 or 0	1 or 0	1	1
(c)	0	0	1 or 0	1 or 0	0	1
(d)	1	1	0	0	0	0
(e)	1	1	1	0	1	0
(f)	1	1	1	1	1	1
(g)	1	1	0	1	1	1

Notes

1. For TV mode (Picture on = 1, Superimpose mode not allowed) rows (a), (d) and (g) of above table refer to display row 0 only. For all other rows text display is disabled and Blanking = 0.
2. The R, G, B outputs may contain character and background colour information. The only exception is that background colours are inhibited when Blanking = 0.



Note: Character Bytes are listed as transmitted from b_1 to b_7

Fig. 4 Character format.

The SAA5051 is identical to the SAA5050 except for the character set (German).

D8241

Bits b_4 b_3 b_2 b_1 / Row	Col 0	Col 1	Col 2	Col 2a	Col 3	Col 3a	Col 4	Col 5	Col 6	Col 6a	Col 7	Col 7a
0 0 0 0 / 0	NUL*	DLE*			0		§	P	°		p	
0 0 0 1 / 1	Alpha Red	Graphics Red	!		1		A	Q	a		q	
0 0 1 0 / 2	Alpha Green	Graphics Green	"		2		B	R	b		r	
0 0 1 1 / 3	Alpha Yellow	Graphics Yellow	#		3		C	S	c		s	
0 1 0 0 / 4	Alpha Blue	Graphics Blue	$		4		D	T	d		t	
0 1 0 1 / 5	Alpha Magenta	Graphics Magenta	%		5		E	U	e		u	
0 1 1 0 / 6	Alpha Cyan	Graphics Cyan	&		6		F	V	f		v	
0 1 1 1 / 7	Alpha** White	Graphics White	'		7		G	W	g		w	
1 0 0 0 / 8	Flash	Conceal Display	(		8		H	X	h		x	
1 0 0 1 / 9	Steady**	Contiguous Graphics**	)		9		I	Y	i		y	
1 0 1 0 / 10	End Box**	Separated Graphics	*		:		J	Z	j		z	
1 0 1 1 / 11	Start Box	ESC*	+		;		K	Ä	k		ä	
1 1 0 0 / 12	Normal Height**	Black Background**	,		<		L	Ö	l		ö	
1 1 0 1 / 13	Double Height	New Background	-		=		M	Ü	m		ü	
1 1 1 0 / 14	SO*	Hold Graphics	.		>		N	^	n		ß	
1 1 1 1 / 15	S1*	Release Graphics**	/		?		O	_	o		■	

Control characters shown in columns 0 and 1 are normally displayed as spaces.

* These control characters are reserved for compatability with other data codes.

** These control characters are presumed before each row begins

Codes may be referred to by their column and row e.g. 2/5 refers to %

☐ Character rectangle

Black represents display colour.

White represents background.

TELETEXT CHARACTER GENERATOR

(SWEDISH)

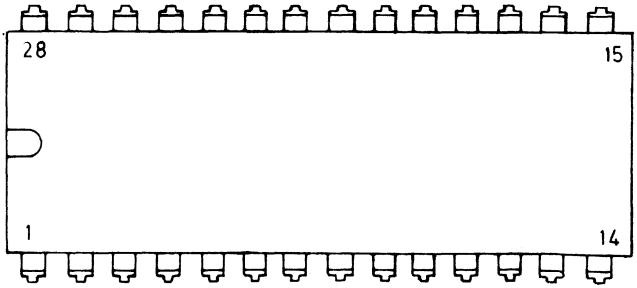
The SAA5052 is an MOS N-channel integrated circuit which provides the video drive signals to the television set necessary to produce the teletext/viewdata display.
The SAA5052 is a 28-pin device which incorporates a fast access character generator ROM (4.3 k bits), the logic decoding for all the teletext control characters and decoding for some of the remote control functions.
The circuit generates 96 alphanumeric and 64 graphic characters. In addition there are 32 control characters which determine the nature of the display.
The SAA5052 is suitable for direct connection to the SAA5010, SAA5020 and SAA5040 integrated circuits.
The SAA5052 provides a Swedish Character Set.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom	5	V
Supply current	I_{DD}	typ	85	mA
Operating ambient temperature	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117)



Viewed from top

Pinning: see next page

PINNING

1. V_{SS}
2. Superimpose
3. Remote control data ($\overline{DATA}$)
4. Character data input 1 (D1)
5. Character data input 2 (D2)
6. Character data input 3 (D3)
7. Character data input 4 (D4)
8. Character data input 5 (D5)
9. Character data input 6 (D6)
10. Character data input 7 (D7)
11. Remote control data clock (DLIM)
12. General line reset ($\overline{GLR}$)
13. Data entry window (DEW)
14. Character rounding select (CRS)
15. Big character select ($\overline{BCS}$)
16. Transmitted large character ($\overline{TLC}$)
17. Not connected
18. V_{DD}
19. 6 MHz Input (TR6)
20. 1 MHz Input (F1)
21. Monochrome video output (Y)
22. Blue output (B)
23. Green output (G)
24. Red output (R)
25. Blanking output
26. Load output shift register enable (LOSE)
27. Picture on input (PO)
28. Display enable input (DE)

DESCRIPTION

The basic input to the SAA5052 is the character data from the teletext page memory. This is a 7 bit code. Each character code defines a dot matrix pattern. The character period is 1 μs and the character dot rate is 6 MHz. The timings are derived from the two external input clocks F1 (1 MHz) and TR6 (6 MHz) which are amplified and re-synchronised internally. Each character rectangle is 6 dots wide by 10 TV lines high. One dot space is left between adjacent characters, and there is one line space left between rows. Alphanumeric characters are generated on a 5 x 9 matrix, allowing space for descending characters. Each of the 64 graphics characters is decoded to form a 2 x 3 block arrangement which occupies the complete 6 x 10 dot matrix (Fig.3). Graphics characters may be either contiguous or separated (Fig.4). The alphanumeric characters are character rounded, i.e. a half dot is inserted before or after a whole dot in the presence of a diagonal in a character matrix.

The character video output signals comprise a monochrome signal and RGB signals for a colour receiver. A blanking output signal is provided to blank out the television video signal when a newsflash or subtitle is to be displayed.

The monochrome data signal can be used to inlay characters into the television video. The use of the 32 control characters provides information on the nature of the display, e.g. colour. These are also used to provide other facilities such as 'concealed display' and flashing words etc. The full character set is given in Table 1.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (See MOS Handling Notes).

RATINGS Limiting values in accordance with the Absolute Maximum System.

		min.	typ.	max.	
Voltages (with respect to pin 1)					
Supply voltage (pin 18)		−0.3	–	7.5	V
Input voltages	All inputs + input/output	−0.3	–	7.5	V
Output voltage (pin 16)		−0.3	–	7.5	V
	All other outputs	−0.3	–	14.0	V
Temperature					
Storage temperature	T_{stg}		−20 to +125		°C
Operating ambient temperature	T_{amb}		−20 to +70		°C

CHARACTERISTICS

Supply voltage		min.	typ.	max.	
V_{DD} (pin 18)		4.5	–	5.5	V

The following parameters apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current					
I_{DD}		–	85	160	mA
Inputs					
Character data D1 to D7 (pins 4–10)					
Input voltage, HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Data set-up time } see Fig.2		150	–	–	ns
Data hold time } see Fig.2		100	–	–	ns
Clock inputs F1 (pin 20) **TR6** (pin 19)					
Input voltage; HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Logic inputs					
$\overline{DATA}$ (pin 3) DEW (pin 13) LOSE (pin 26)					
DLIM (pin 11) $\overline{CRS}$ (pin 14) PO (pin 27)					
$\overline{GLR}$ (pin 12) $\overline{BCS}$ (pin 15) DE (pin 28)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
All inputs					
Input leakage (V_{in} 5.5 V)		–	–	10	μA
Input capacitance		–	–	7	pF

CHARACTERISTICS (continued)

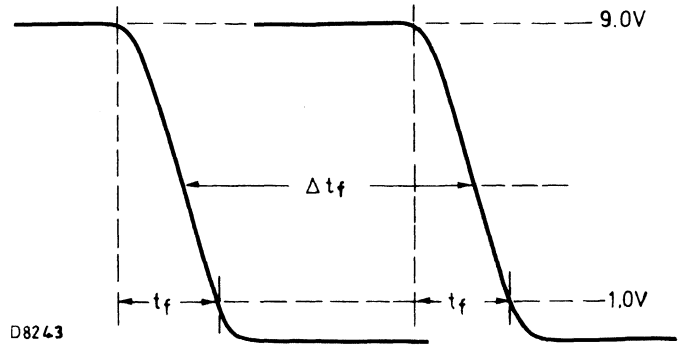
		min.	typ.	max.	
Outputs					
Character video outputs + Blanking output (Open drain)					
B - (pin 22), G - (pin 23), R - (pin 24), Y - (pin 21), Blanking (pin 25)					
Output voltage; LOW (I_{OL} = 2 mA)	V_{OL}	–	–	0.5	V
Output voltage; LOW (I_{OL} = 4 mA)		–	–	1.0	V
Output voltage; LOW (I_{OL} = 6 mA)		–	–	2.0	V
Output voltage; HIGH	V_{OH}	V_{DD}	–	13.2	V
Output load capacitance		–	–	15	pF
Output fall time t_f (Note 1)		–	–	30	ns
Variation of fall time between any outputs Δt_f (Note 1)		0	–	20	ns
$\overline{\text{TLC}}$ (pin 16)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		–	–	30	pF
Output rise time (Measured between 0.8 V and 2.0 V levels)		–	–	1.0	μs
Output fall time (Measured between 0.8 V and 2.0 V levels)		–	–	1.0	μs
Input/output					
$\overline{\text{Superimpose}}$ (pin 2) (Open drain)					
Input voltage; HIGH	V_{IH}	2.0	–	6.5	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input leakage (V_{in} = 5.5 V)		–	–	10	μA
Input capacitance		–	–	7	pF
Output voltage; LOW (I_{OL} = 0.4 mA)	V_{OL}	0	–	0.5	V
Output voltage; LOW (I_{OL} = 1.3 mA)	V_{OL}	0	–	1.0	V
Output load capacitance		–	–	45	pF
Output voltage; HIGH state (Note 2)	V_{OH}	–	–	6.5	V

Notes

1. Fall time, t_f and Δt_f, are defined as shown and are measured using the circuit shown below:

   t_f is measured between the 9 V and 1 V levels.

   Δt_f is the maximum time difference between outputs.



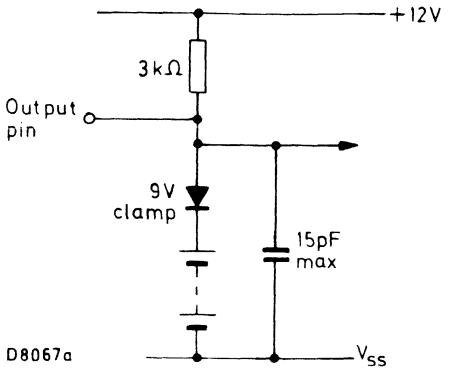


Fig.1

2. Recommended pull-up resistor for $\overline{\text{Superimpose}}$ is 18 kΩ.
3. The R,G,B,Y and blanking outputs are protected against short circuit to supply rails.

SPECIAL FEATURES

Flash oscillator

The circuit generates a 0.75 Hz signal with a 3:1 ON/OFF ratio to provide the flashing character facility.

Power-on-reset

When the supply voltage is switched on, the character generator will reset to TV, conceal and not superimpose modes.

SPECIAL FEATURES (continued)

Character rounding

The character rounding function is different for the small and double height characters. In both cases the ROM is accessed twice during the character period of 1 μs. The dot information of two rows is then compared to detect the presence of any diagonal in the character matrix and to determine the positioning of the character rounding half dots.
For small characters rounding is always referenced in the same direction (i.e. row before in even fields and row after in odd fields as determined by the CRS signal).
For double height characters rounding is always referenced alternately up and down changing every line using an internally generated signal. (The CRS signal is '0' for the odd field and '1' for the even field of an interlaced TV picture).

Graphics decoder

The 64 graphics characters are decoded directly from the character data inputs and they appear on a 2 x 3 matrix. Figure 3 gives details of the graphics decoding.

APPLICATION DATA

The function is quoted against the corresponding pin numbers

Pin No.

1. V_{SS} Ground - 0 V

2. **$\overline{\text{Superimpose}}$**

   This is a dual purpose input/output pin. The output is an open drain transistor (capable of sinking current to V_{SS}), which is in the conducting state when superimpose mode is selected. This allows contrast reduction of the TV picture in superimpose mode if required. If the pin is held low, the internal 'TV mode' flip-flop is held in the 'text' state. This is for VDU applications when the remote control is not used.

3. **$\overline{\text{DATA}}$ Remote control data**

   This input accepts a 7-bit serial data stream from the SAA5010 remote control receiver decoder. This data contains the teletext and viewdata remote control user functions. The command codes used in the SAA5052 are shown in Table 2.

4, 5, 6, 7, 8, 9, 10. **Character data D1 to D7**

   These inputs accept a 7-bit parallel data code from the page memory. This data selects the alphanumeric characters, the graphics characters and the control characters. The alphanumeric addresses are ROM column addresses, the graphics and control data are decoded internally.

11. **DLIM**

    This input receives a clock signal from the SAA5010 remote control receiver decoder. This signal is used to clock remote control data from the SAA5010 into the remote control data input (Pin 3).

12. **$\overline{\text{GLR}}$ General line reset**

    This input signal from the SAA5020 Timing Chain is required for internal synchronisation of remote control data signals.

13. **DEW Data entry window**

    This input signal from the SAA5020 Timing Chain is required to reset the internal ROM row address counter prior to the display period. It is also used internally to derive the 'flash' period.

14. **CRS Character rounding select**

This input signal from the SAA5020 Timing Chain is required for correct character rounding of displayed characters. (Normal height characters only).

15. **$\overline{\text{BCS}}$ Big character select**

This input from the SAA5040 Teletext Acquisition and Control device allows selection of large characters by remote control.

16. **$\overline{\text{TLC}}$ Transmitted large characters**

This output to the SAA5020 Timing Chain enables double height characters to be displayed as a result of control characters stored in the page memory.

18. **V_{DD} + 5 V supply**

This is the power supply input to the circuit.

19. **TR6**

This input is a 6 MHz signal from the SAA5020 Timing Chain used as a character dot rate clock.

20. **F1**

This input is a 1 MHz equal mark/space ratio signal from the SAA5020 Timing Chain. It is used to latch the 7-bit parallel character data into the input latches. It is also used to synchronise an internal divide-by 6 counter. The F1 signal is internally synchronised with TR6.

21. **Y Output (Monochrome)**

This is a video output signal which is active in the high state containing character dot information for TV display.
The output is an open drain transistor capable of sinking current to V_{SS}.

22, 23, 24 **Blue, Green, Red outputs**

These are the Blue, Green and Red Character video outputs to the TV display circuits. They are active high and contain both character and background colour information.
The outputs are open drain transistors capable of sinking current to V_{SS}.

25. **Blanking**

This active high output signal provides TV picture video blanking. It is active for the duration of a box when Picture on and Display enable are high. It is also activated permanently for normal teletext display when no TV picture is required (PO low). The output is an open drain transistor capable of sinking current to V_{SS}. Full details given in Table 3.

26. **LOSE Load output shift register enable**

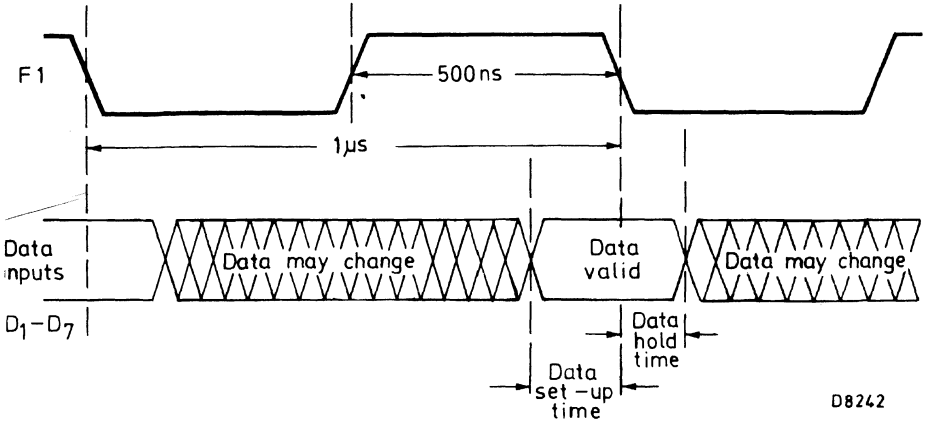
This input signal from the SAA5020 Timing Chain resets the internal control character flip-flops prior to the start of each display line.
This signal also defines the character display period.

27. **PO Picture on**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to control the character video and blanking outputs. When PO is high, only text in boxes is displayed unless in superimpose mode. The input is high for TV picture video on, low for picture off. See Table 3.

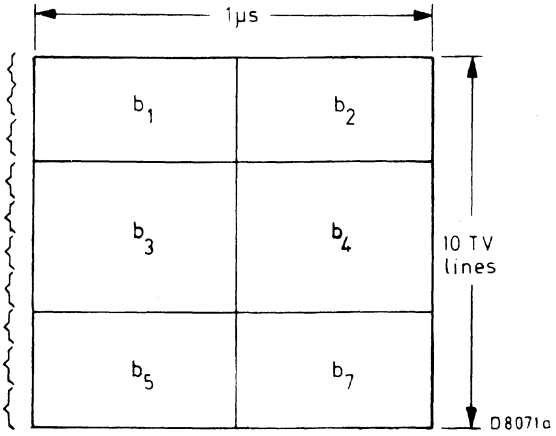
28. **DE Display enable**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to enable the teletext display. The input is high for teletext display enabled, low for display cancelled. See Table 3.



Note: All timings measured at 1.5 V level.

Fig. 2 Data input timing.



Each cell is illuminated if particular 'bit' (b_1, b_2, b_3, b_4, b_5, or b_7) is a '1'.

For graphics characters b_6 is always a 1 - See Table 1.

Fig. 3 Graphics Character.

SAA5052 CHARACTER SET

D8241

Bits b_4 b_3 b_2 b_1	Row	Col 0	Col 1	Col 2	Col 2a	Col 3	Col 3a	Col 4	Col 5	Col 6	Col 6a	Col 7	Col 7a
0 0 0 0	0	NUL *	DLE *	☐	☐	Ø	▄	É	P	é	▄	p	▄
0 0 0 1	1	Alpha Red	Graphics Red	!	▀	1	▀	A	Q	a	▀	q	▀
0 0 1 0	2	Alpha Green	Graphics Green	"	▀	2	▀	B	R	b	▀	r	▀
0 0 1 1	3	Alpha Yellow	Graphics Yellow	#	▀	3	▀	C	S	c	▀	s	▀
0 1 0 0	4	Alpha Blue	Graphics Blue	¤	▀	4	▀	D	T	d	▀	t	▀
0 1 0 1	5	Alpha Magenta	Graphics Magenta	%	▀	5	▀	E	U	e	▀	u	▀
0 1 1 0	6	Alpha Cyan	Graphics Cyan	&	▀	6	▀	F	V	f	▀	v	▀
0 1 1 1	7	Alpha White **	Graphics White	'	▀	7	▀	G	W	g	▀	w	▀
1 0 0 0	8	Flash	Conceal Display	(	▀	8	▀	H	X	h	▀	x	▀
1 0 0 1	9	** Steady	** Contiguous Graphics	)	▀	9	▀	I	Y	i	▀	y	▀
1 0 1 0	10	** End Box	Separated Graphics	*	▀	:	▀	J	Z	j	▀	z	▀
1 0 1 1	11	Start Box	* ESC	+	▀	;	▀	K	Ä	k	▀	ä	▀
1 1 0 0	12	** Normal Height	** Black Background	,	▀	<	▀	L	Ö	l	▀	ö	▀
1 1 0 1	13	Double Height	New Background	-	▀	=	▀	M	Å	m	▀	å	▀
1 1 1 0	14	* SO	Hold Graphics	.	▀	>	▀	N	Ü	n	▀	ü	▀
1 1 1 1	15	* SI	** Release Graphics	/	▀	?	▀	O	_	o	▀	■	▀

Control characters shown in columns 0 and 1 are normally displayed as spaces.

* These control characters are reserved for compatability with other data codes.

** These control characters are presumed before each row begins

Codes may be referred to by their column and row e.g. 2/5 refers to %

☐ Character rectangle

Black represents display colour.

White represents background.

Table 1

TABLE 2

Remote control command codes used in the SAA5052

CODE b_7	b_6	b_5	b_4	b_3	b_2	b_1	COMMAND	FUNCTION
0	X	X	X	X	X	X	'TV' mode	Allows text on top row of display only.
1	X	X	X	X	X	X	'Text' mode	Allows text throughout display period.
1	0	1	1	1	1	0	Superimpose	Sets superimpose mode.
1	0	1	1	1	1	1	Teletext	Resets superimpose mode.
0	X	X	X	X	X	X	'TV' mode	Resets superimpose mode.
1	1	X	X	X	X	X	Viewdata mode.	Resets superimpose mode.
1	X	0	0	1	1	0	Reveal	Reveals for time-out (notes 3, 4).
1	X	0	1	0	1	1	Reveal set	Sets reveal mode (note 3).
Any command apart from reveal set.								Resets reveal mode (note 3).

X = Don't care.

Notes

1. When the power is applied the SAA5052 is set into the 'TV' mode and reset out of superimpose and reveal modes.
2. 'Text' mode is selected when the $\overline{\text{superimpose}}$ pin is held low.
3. Reveal mode allows display of text previously concealed by 'conceal display' control characters.
4. This code is sent from the SAA5010 as a repeated command. Thus reveal mode is set for as long as the reveal key is depressed. The SAA5052 reverts to normal 'not reveal' mode 160 ms after the last reveal command.
5. The superimpose output is low only if superimpose mode is set and the DE (display enable) input is high.
6. The above table shows code required for functions specified.
   The SAA5010 transmits and the SAA5052 requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$ $\overline{b_1}$ $\overline{b_2}$ $\overline{b_3}$ $\overline{b_4}$ $\overline{b_5}$ $\overline{b_6}$. For full details of remote control data coding see SAA5010 data sheet.

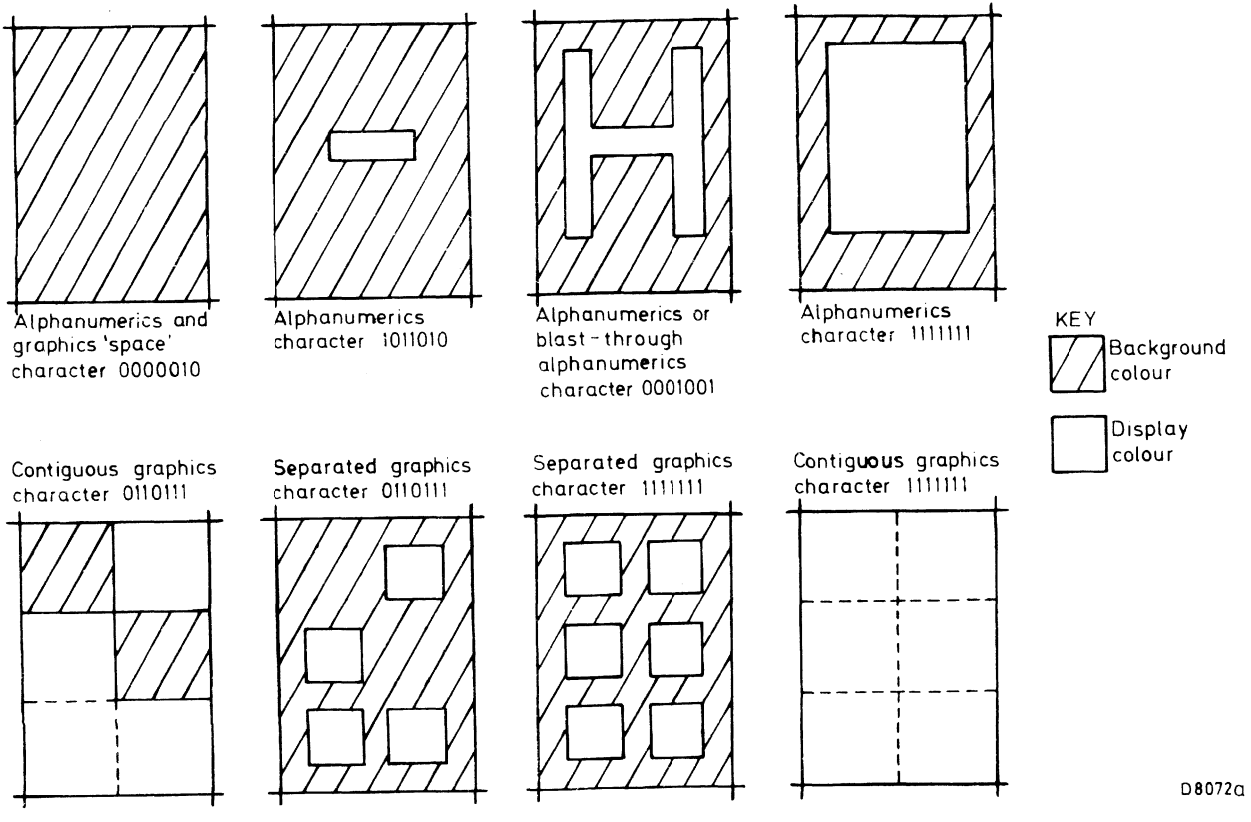
TABLE 3

Conditions affecting display

	Inputs		Control data		Outputs	
	Picture On (PO)	Display Enable (DE)	Superimpose Mode	Box	Text Display Enabled (i.e. R, G, B, Y outputs)	Blanking
(a)	1	0	1 or 0	1 or 0	0	0
(b)	0	1	1 or 0	1 or 0	1	1
(c)	0	0	1 or 0	1 or 0	0	1
(d)	1	1	0	0	0	0
(e)	1	1	1	0	1	0
(f)	1	1	1	1	1	1
(g)	1	1	0	1	1	1

Notes

1. For TV mode (Picture on = 1, Superimpose mode not allowed) rows (a), (d) and (g) of above table refer to display row 0 only. For all other rows text display is disabled and Blanking = 0.
2. The R, G, B outputs may contain character and background colour information. The only exception is that background colours are inhibited when Blanking = 0.



Note: Character Bytes are listed as transmitted from b_1 to b_7

Fig. 4 Character format.

SUPERSEDES DATA SHEET SAB1009A AUGUST 1978

WIDE-BAND LIMITING AMPLIFIER

The SAB1009B is a three-stage differential amplifier in the range 70 to 900 MHz with inherent limiting action. The differential inputs are internally biased to permit capacitive coupling and asymmetrical drive. For asymmetrical drive pin 3 should be used as an input and pin 4 should be grounded via a 56 Ω resistor and a d.c. blocking capacitor. The outputs are complementary with non-standard levels.
The device is specified for a nominal supply voltage of 5 V; it may also be operated with a supply voltage of 5,2 V ± 5%. The voltage dropping resistor R_{CC} has then to be increased to 82 Ω.

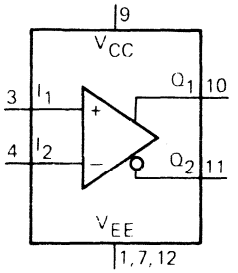


Fig. 1 Block diagram.

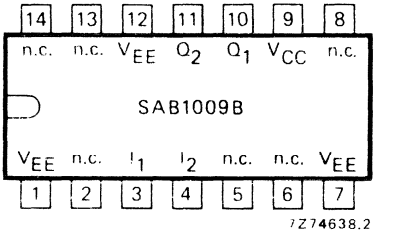


Fig. 2 Pins marked n.c. should preferably be grounded or connected to supply.
V_{CC} via 75 Ω to 5 V.
V_{EE} = 0 V (ground).

QUICK REFERENCE DATA

Supply voltage	V_{CC}		5 ± 5% V
Supply voltage dropping resistor	R_{CC}		75 Ω
Frequency range	f_i		70 to 900 MHz
Differential clipped output voltage R_L = 50 Ω at each output	$V_{o(p-p)}$	typ.	550 mV
Power consumption per package (no load)	P_{av}	typ.	75 mW
Operating ambient temperature	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

14-lead DIL; plastic (SOT-27S, T, V).

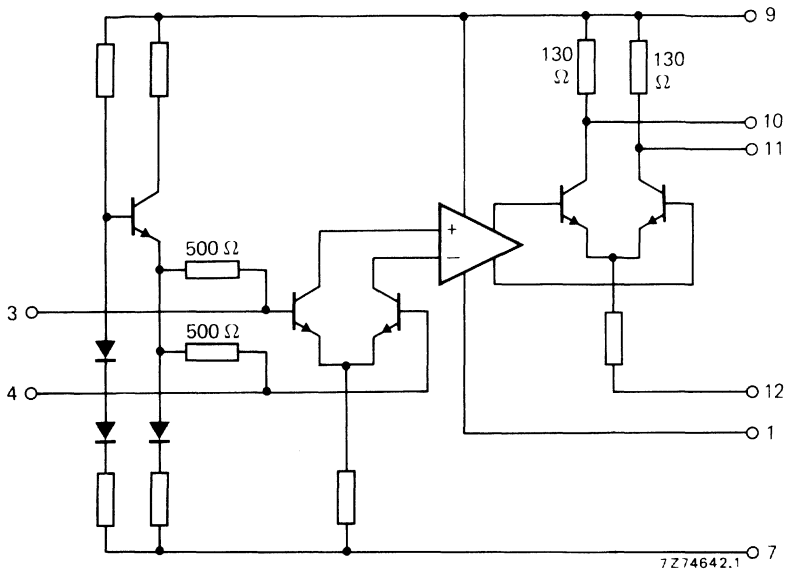


Fig. 3 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7	V
Input voltage	V_I		0 to + 5	V
Storage temperature	T_{stg}		−55 to + 125	°C
Junction temperature	T_j	max.	125	°C

DEVELOPMENT SAMPLE DATA

D.C. CHARACTERISTICS

V_{CC} via 75 Ω to 5 V

The circuit has been designed to meet the d.c. specifications shown in the table below after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

	symbol	pin under test	T_{amb} (°C) 0	25	70		conditions
Supply current	I_{CC} typ.	9	–	23	–	mA	pins 3 and 4 open, no d.c. load.
	I_{CC} max.		–	30	–	mA	

A.C. CHARACTERISTICS

V_{CC} via 75 Ω to 5 V ± 5%; T_{amb} = 0 to + 70 °C

	symbol	pin under test	min.	typ.	max.		conditions
Frequency range	f_i		70	–	900	MHz	
Gain *	G		26	–	–	dB	f_i = 70 MHz
			26	–	–	dB	f_i = 100 MHz
			23	–	–	dB	f_i = 200 MHz
			19	–	–	dB	f_i = 500 MHz
			16	–	–	dB	f_i = 900 MHz
Gain variation versus temperature	ΔG		–	–	1,5	dB	
Input voltage standing-wave ratio	VSWR	3	–	–	5		$V_{i(rms)}$ = 25 mV; $Z_{i\,nom}$ = 75 Ω Source connected to pin 3; pin 4 grounded via 56 Ω in series with 10 nF.
Input voltage	$V_{i(rms)}$	3	–	–	150	mV	

* For gain definition see Fig. 6 ($G = 20 \log \frac{V_2}{V_1}$).

A.C. CHARACTERISTICS (continued)

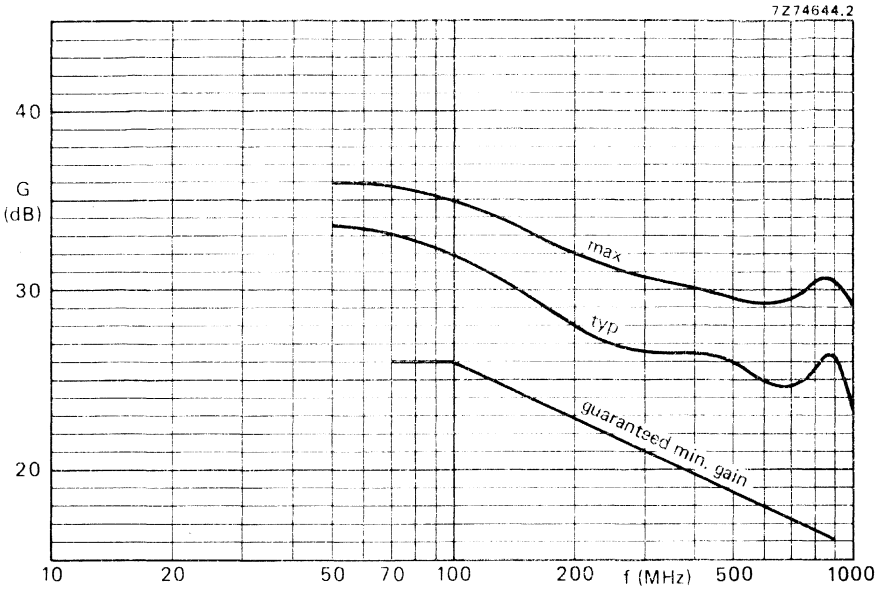
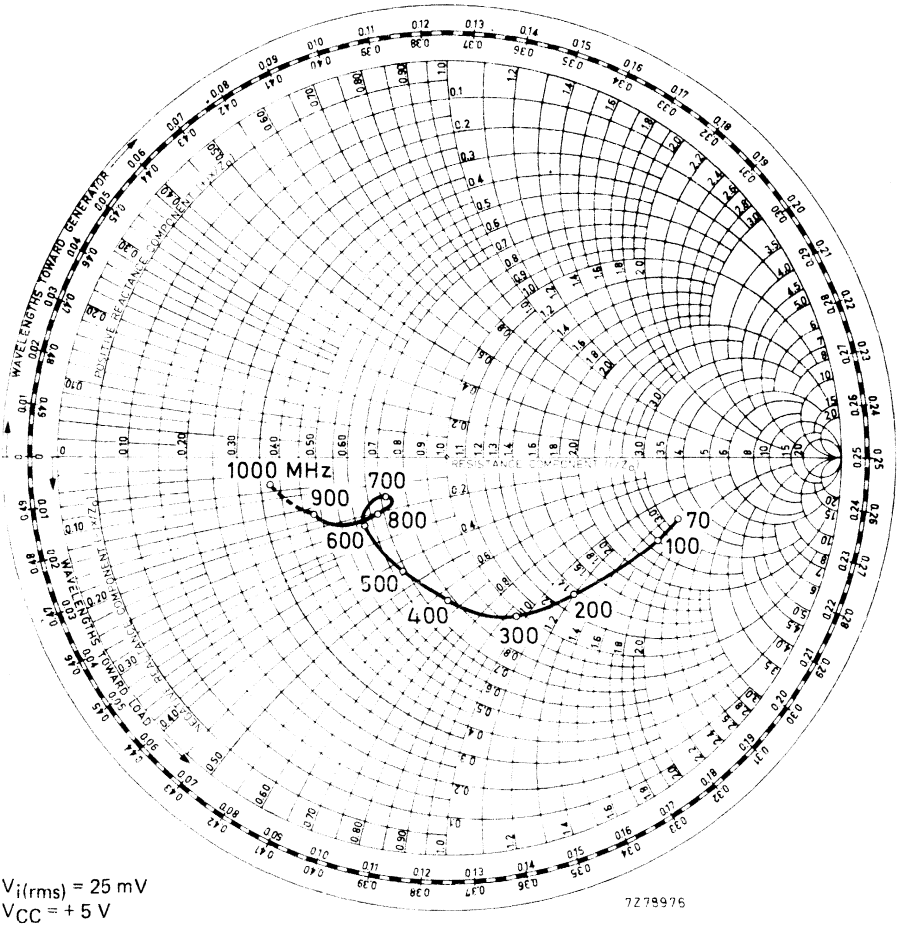


Fig. 4 Gain as a function of frequency. V_{CC} = 5 V; T_{amb} = 25 °C.

A.C. CHARACTERISTICS (continued)



$V_{i(rms)}$ = 25 mV
V_{CC} = + 5 V
R_{CC} = 75 Ω

Fig. 5 Smith chart of typical input impedance at pin 3 with pin 4 terminated to ground.

Test circuit

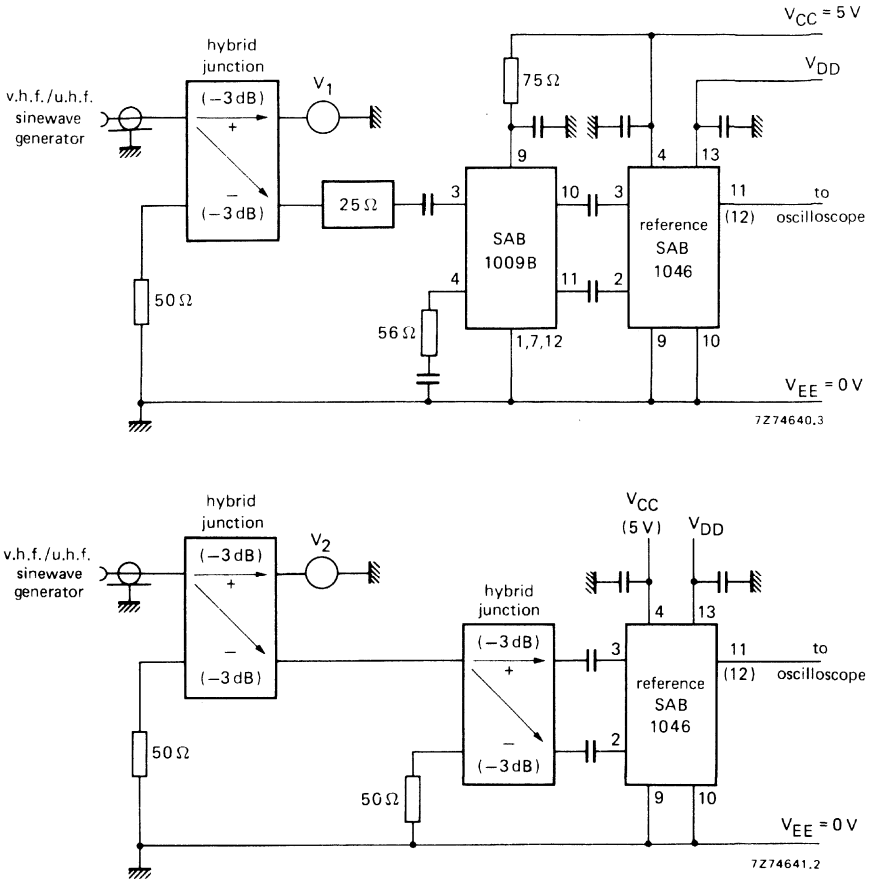


Fig. 6 Test circuits for defining gain.

V_1 and V_2 are minimum input levels for correct operation.

Gain defined as $G = 20 \log \frac{V_2}{V_1}$.

Capacitors must be leadless ceramic (value 10 nF).
Hybrid junctions are Anzac H-183-4 or similar.
Connections to the device must be kept short for proper tests.
Cables are 50 Ω coaxial cables.

APPLICATION INFORMATION

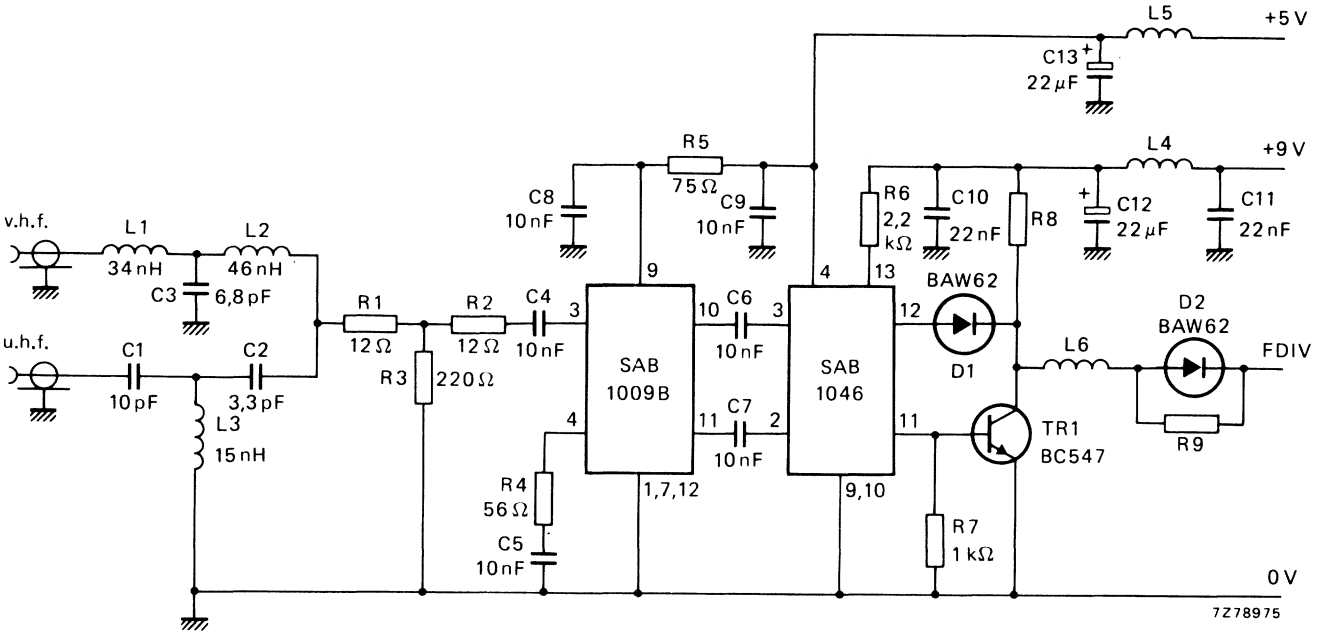


Fig. 7 H.F. divider for DICS in television receivers (prescaler module). The pins not mentioned are connected to ground except pin 5 of SAB1046 which is connected to V_{CC}. Values of R8, R9 and L6 have to be chosen in accordance with the load capacitance.

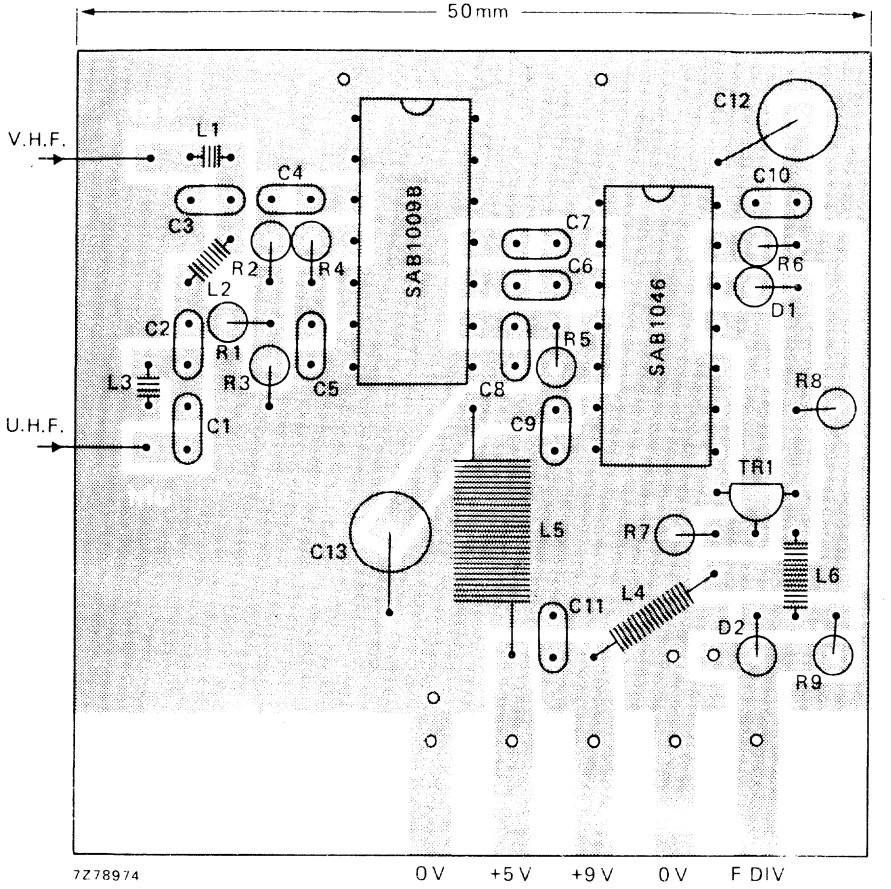


Fig. 8 Component layout of circuit shown in Fig. 7.

CONTROL CIRCUIT FOR ON-SCREEN DISPLAY OF STATION AND/OR CHANNEL NUMBER

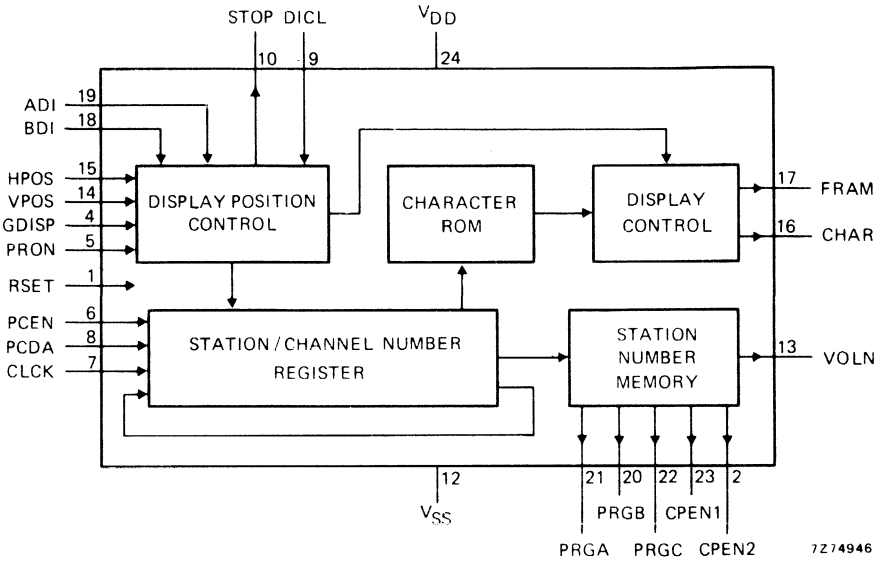


Fig. 1 Block diagram.

Features

- Station and channel number display (4 digits).
- Station number display is separate (2 digits; 1 to 16).
- 4-digit display (00 00 to 99 99).
- Character rounding for improving the legibility of the numerals.
- Internal digital display positioning and defining the length of display; no control knob.
- Control signal for separate background.
- Parallel outputs for station information.

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	8 to 10	V
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Input frequency	f_{DICL}	typ. 2,5	MHz
Clock frequency	f_{CLCK}	typ. 62,5	kHz
Quiescent current; V_{DD} = 10 V; I_Q = 0; T_{amb} = 25 °C	I_{DD}	typ. 20	μA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The SAB1016 integrated circuit controls the on-screen display of station and/or channel number. It generates data for partially blanking the upper part of the scan of a TV receiver and thereby displaying the number of the selected station and/or channel. The numerals are normally displayed for 2,5 seconds after station/channel selection.

Modes of operation:

- flashing display facility during store
- background only if channel mode is set, or in search tuning mode
- persistent on-screen display

The 4 characters are presented on a background; station number left and channel number right, separated by a blank position.

The characters are built up from a 5 x 7 dot matrix. The duration of one display data bit is $\approx$ 400 ns in the horizontal direction; vertically a display data bit corresponds to 3 lines per half picture. The legibility of the display is improved by incorporation of the additional display rounding facility; i.e. display dots which were touching diagonally are now connected by an extra display rounding dot, which is displaced by half a dot horizontally and one line per half picture vertically.

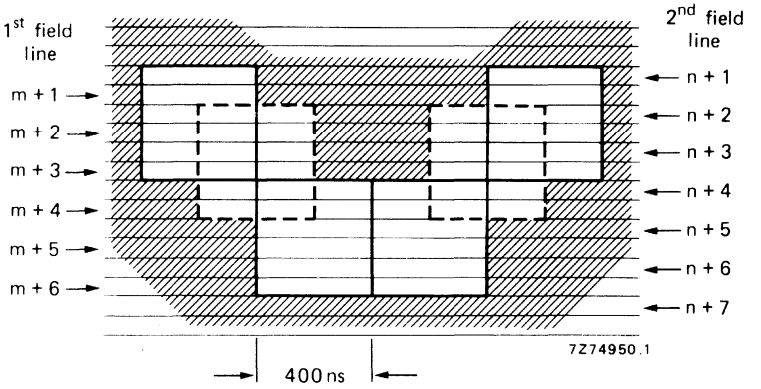


Fig. 2 Construction of a character from display dots with additional character rounding dots.

OPERATION DESCRIPTION

Data input

The data input for generation of the characters is performed serially via the data input PCDA — synchronized with the system clock (CLCK). The data are accepted if, during data transfer, the data enable input PCEN is HIGH. The data are accepted into an input register, which also serves as a shift register. In order to represent 4 characters, a group of 16 bits is necessary as the address for the internal 12 x 36-bit character ROM. The following characters are displayed on the screen according to the code in Table 1.

Table 1

address code				on-screen selected character
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	:
1	0	1	1	blank
1	1	0	0	blank
1	1	0	1	blank
1	1	1	0	blank
1	1	1	1	blank

The positioning of the on-screen display and the number of digits are controlled by the logic states at the control inputs GDISP and PRON (see Table 2). They also define the display format of the commands accepted by the circuit (see Fig. 4).

Table 2. Display format

control inputs		display format	DBUS format	display format
GDISP	PRON			
0	0	6 bits	IBUS	2 digit; station no. at left (1 to 16)
0	1	16 bits	GBUS	4 digit; e.g. clack (00 00 to 99 99)
1	0	6 bits	IBUS	2 digit; station no. at right (1 to 16)
1	1	13 bits	DBUS	4 digit; station and/or channel no. at right (1 to 16 99)

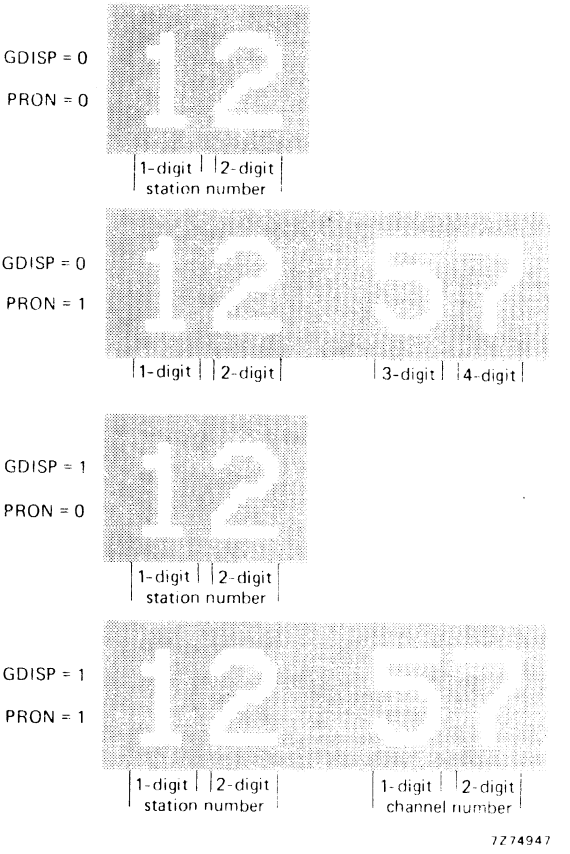


Fig. 3 Presentation of the various display formats.

The various data words have different lengths and conform to the following formats:

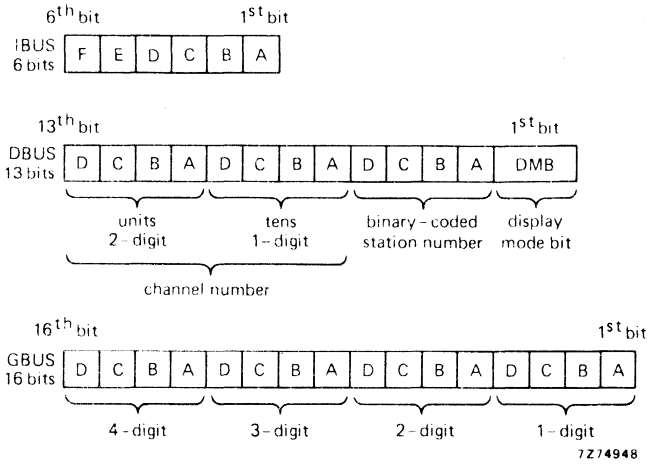


Fig. 4 Available display formats. A start bit is sent before each data word in each case.

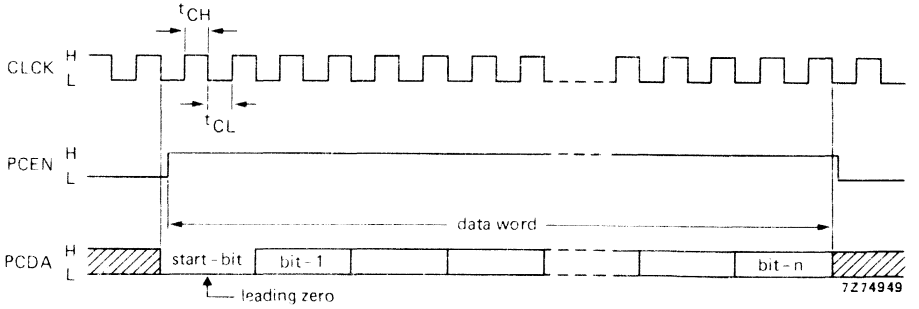


Fig. 5 Display data timing diagram.

Data word IBUS

The serial transfer of the 6-bit IBUS data word is accepted on input PCDA, when input PRON is LOW, and the data contain the control and display instructions as given in Table 3.

Table 3. IBUS instructions

	IBUS code						instruction
	F	E	D	C	B	A	
2	0	0	0	0	1	0	off (stand by)
4	0	0	0	1	0	0	display short (2,5 s)
16	0	1	0	0	0	0	station 16
17	0	1	0	0	0	1	1
18	0	1	0	0	1	0	2
19	0	1	0	0	1	1	3
20	0	1	0	1	0	0	4
21	0	1	0	1	0	1	5
22	0	1	0	1	1	0	6
23	0	1	0	1	1	1	7
24	0	1	1	0	0	0	8
25	0	1	1	0	0	1	9
26	0	1	1	0	1	0	10
27	0	1	1	0	1	1	11
28	0	1	1	1	0	0	12
29	0	1	1	1	0	1	13
30	0	1	1	1	1	0	14
31	0	1	1	1	1	1	15
32	1	0	0	0	0	0	display on/off
36	1	0	0	1	0	0	step station up
37	1	0	0	1	0	1	step station down

Any possible input codes which are not in Table 3 will be received by the circuit, but not evaluated. The station number, transmitted in binary form, will be transferred internally into a 2 x 4 bit code (BCD).

The display mode control inputs ADI and BDI must be connected to LOW.

Data word DBUS

The serial transfer of the 13-bit DBUS data word is arranged as a display mode bit (DMB) together with 3 data blocks, and is accepted according to the conditions of Table 2. Bits 2 to 5 contain station numbers 1 to 16, which are transferred into 2 x 4 bits internally; whilst bits 7 to 9 and 10 to 13 contain the 1st and 2nd digit of the channel number respectively; they are binary coded as given in Table 4.

Table 4. Specification of the DBUS code

DBUS input code				channel number	station number
D	C	B	A		
0	0	0	0	0	16
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	:	10
1	0	1	1	blank	11
1	1	0	0	blank	12
1	1	0	1	blank	13
1	1	1	0	blank	14
1	1	1	1	blank	15

The 1st bit of a DBUS instruction (DMB) is a display mode bit with the following code:

DMB	instruction
0	display of station and channel number
1	display of channel number only

The display mode control inputs ADI and BDI can be driven as required (see Table 5).

Data word GBUS

Corresponding with the input conditions for the control inputs GDISP and PRON quoted in Table 2, the SAB1016 accepts a 17-bit serial data transfer which causes the display of a 4-digit character combination. This is obtained with the GBUS data word. Each part of the four 4-bit data block (see Fig. 4) corresponds with a character, which is binary coded as in Table 1.

Control of display mode

The type and manner of the display can be controlled at the inputs ADI and BDI. The following display modes are provided:

Table 5.

ADI	BDI	display mode
1	0	ON for 2,5 s after selection
0	1	persistent
0	0	flashing (0,32 s ON; 0,32 s OFF)
→ 1	1	background only (2,5 s)

Synchronization

Display synchronization is achieved by means of the inputs VPOS for vertical and HPOS for the horizontal sync. If the sync pulses of a TV correspond with the requirements in Fig. 6, they can be applied directly to the inputs of the circuit.

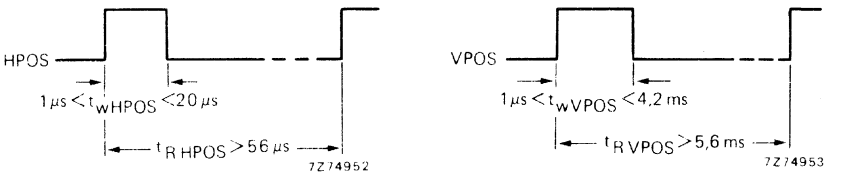


Fig. 6 Sync pulse specifications.

As soon as there is a display command in the form of data received, an external oscillator is started by signal STOP = LOW, which is caused by the first horizontal pulse (HPOS) after a vertical pulse (VPOS). The oscillator frequency is 2,5 MHz, i.e. a periodic time of T = 400 ns, which is the smallest time unit in the representation of a display data bit. The oscillator is stopped at the end of a line.

The instant of time of a display, i.e. the output of signals at FRAM for the background and CHAR for characters is determined by:

1. The state of an internal vertical position counter, which releases the output in the 46th line of a TV picture.
2. The state of the horizontal position counter, which determines the position of the start and finish of display in a picture-line. The display depends on the logic states of the display format control inputs GDISP and PRON (see Fig. 7). The height of the display field (33 lines) and character height (21 lines) are established by the vertical position counter.

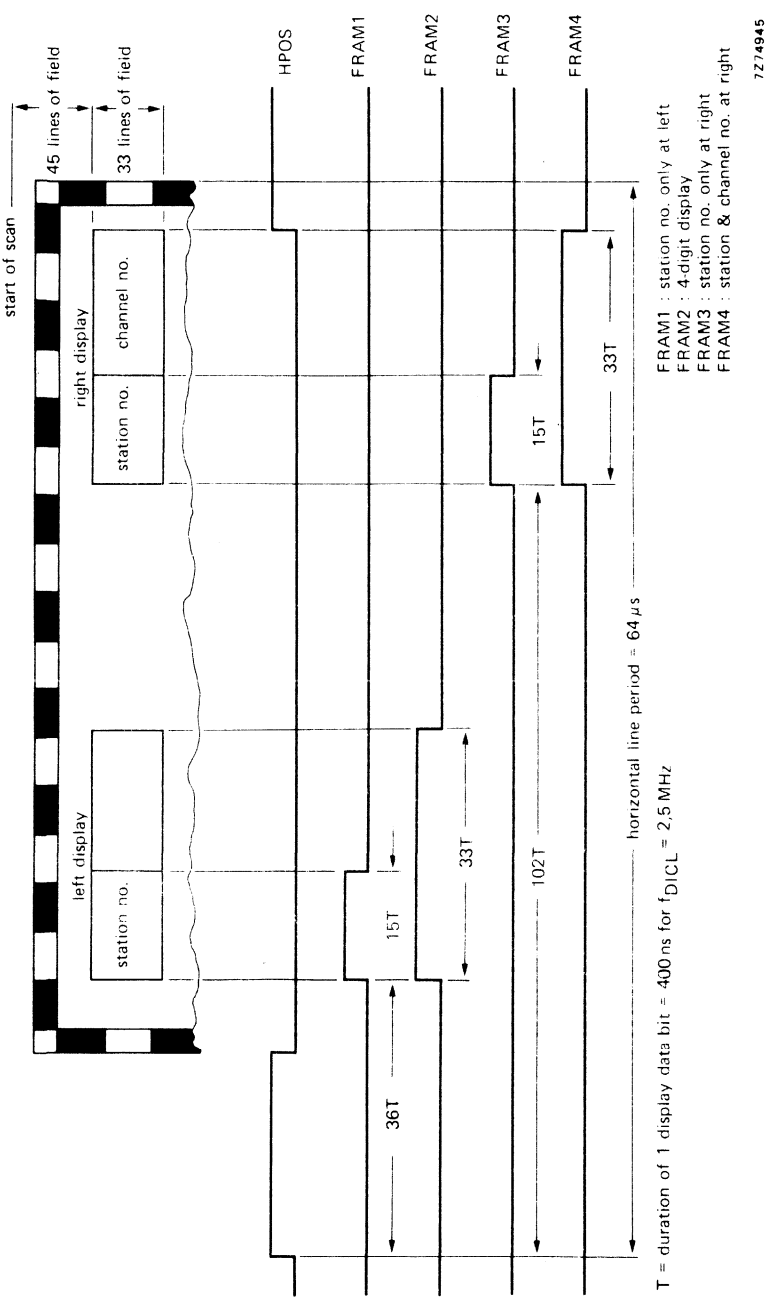


Fig. 7 Relationship between the horizontal pulses from the receiver and the display width defining pulses (FRAM) determined by the display mode inputs GDISP and PRON (see also Table 2).

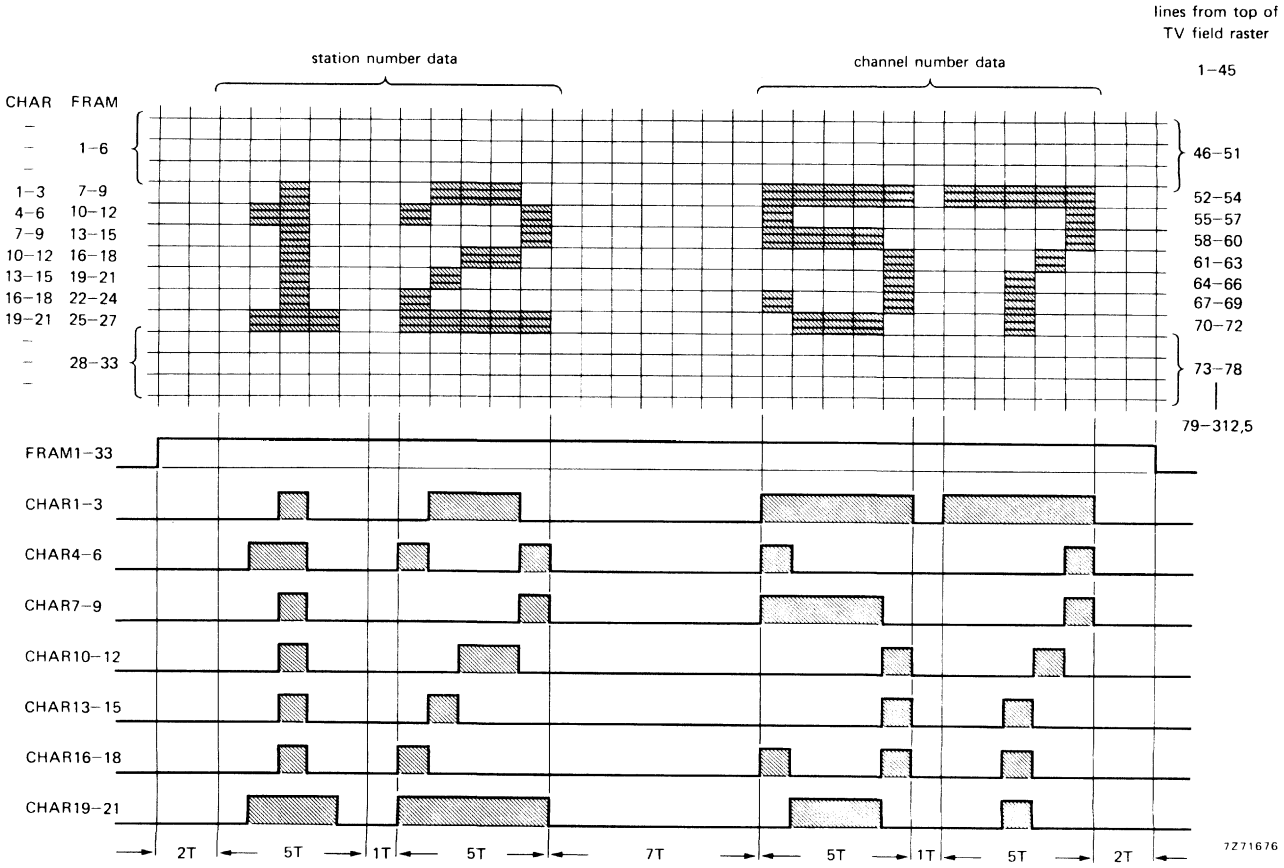


Fig. 8 Display data from the SAB1016. The character rounding bits are omitted for clarity. T = 1 bit duration = 400 ns.

Station memory

Serially transmitted station numbers (DBUS; IBUS) are loaded into the internal station number memory. The output information is available at the station outputs according to Table 6. If an IBUS instruction directs a step station up (+) or down (−), then the setting of the station counter is increased or decreased by 1. The output states at the station outputs also change accordingly.

Table 6.

station no. on display	station outputs				
	CPEN1	CPEN2	PRGC	PRGB	PRGA
01	0	1	0	0	1
02	0	1	0	1	0
03	0	1	0	1	1
04	0	1	1	0	0
05	0	1	1	0	1
06	0	1	1	1	0
07	0	1	1	1	1
08	0	1	0	0	0
09	1	0	0	0	1
10	1	0	0	1	0
11	1	0	0	1	1
12	1	0	1	0	0
13	1	0	1	0	1
14	1	0	1	1	0
15	1	0	1	1	1
16	1	0	0	0	0

After the end of station selection, a HIGH signal appears at output VOLN for 160 ms. This signal can be used for suppression of sound in the TV receiver (muting circuit).

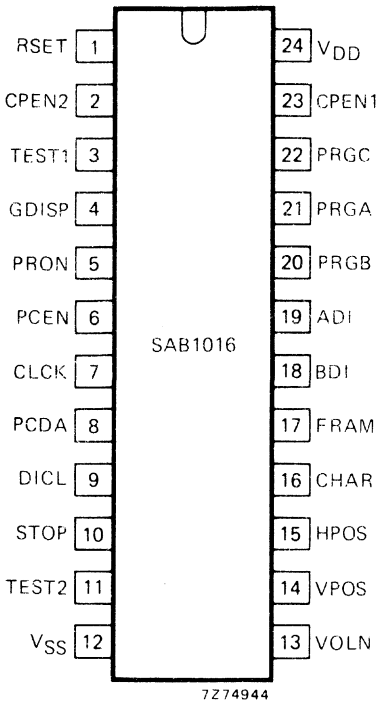


Fig. 9 Pinning diagram.

PINNING

24	V_{DD}	positive supply
12	V_{SS}	negative supply (0 V)

Inputs

1	RSET	reset signal, synchronized internally with system clock
4	GDISP	control of display data format/
5	PRON	position of display field
6	PCEN	data enable (DBUS)
7	CLCK	system clock; 62,5 kHz
8	PCDA	data (DBUS)
9	DICL	display clock; 2,5 MHz
14	VPOS	vertical sync pulse
15	HPOS	horizontal sync pulse
18	BDI	display mode control
19	ADI	display mode control
3	TEST1	test inputs
11	TEST2	test inputs

Outputs

10	STOP	control signal external 2,5 MHz display oscillator
13	VOLN	output signal for muting
16	CHAR	character data output
17	FRAM	display field output (background)
2	CPEN2	station register outputs
20	PRGB	station register outputs
21	PRGA	station register outputs
22	PRGC	station register outputs
23	CPEN1	station register outputs

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 11	V
Input voltage range	V_I	−0,3 to V_{DD} + 0,3	V
Input current	$\pm I_I$	max. 10	mA
Output current	$\pm I_O$	max. 10	mA
Power dissipation per output	P_O	max. 50	mW
Total power dissipation per package	P_{tot}	max. 500	mW
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	8	9	10	V	
Quiescent current per package	10	I_{DD}	–	–	100	µA	I_O = 0; T_{amb} = 25 °C
Input leakage current	10	I_{IR}	–	–	1	µA	all inputs at 10 V; T_{amb} = 25 °C
input leakage current	10	$-I_{IR}$	–	–	1	µA	all inputs at V_{SS}; T_{amb} = 25 °C
Input voltage LOW	8 to 10	V_{IL}	0	–	1,5	V	
Input voltage HIGH	8 to 10	V_{IH}	V_{DD}−1,5	–	V_{DD}	V	
Outputs PRGA,PRGB, PRGC,CPEN1,CPEN2, VOLN							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}−1	–	–	V	$-I_{OH}$ = 1 mA
output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_{OL} = 1 mA
Outputs FRAM,CHAR, STOP							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}−1	–	–	V	$-I_{OH}$ = 3 mA
output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_{OL} = 3 mA
Input DICL							
input frequency	8 to 10	f_{DICL}	–	2,5	2,8	MHz	
duty factor	8 to 10	δ	0,45	–	0,55	–	
rise/fall time	8 to 10	t_r; t_f	–	–	50	ns	
Input CLCK							
input frequency	8 to 10	f_{CLCK}	–	–	100	kHz	
duty factor	8 to 10	δ	0,2	–	0,8		
rise/fall time	8 to 10	t_r; t_f	–	–	1	µs	
Input HPOS							
input frequency	8 to 10	f_{HPOS}	–	–	16	kHz	
rise/fall time	8 to 10	t_r; t_f	–	–	500	ns	
Input VPOS							
input frequency	8 to 10	f_{VPOS}	–	–	100	Hz	
rise/fall time	8 to 10	t_r; t_f	–	–	500	ns	

APPLICATION INFORMATION

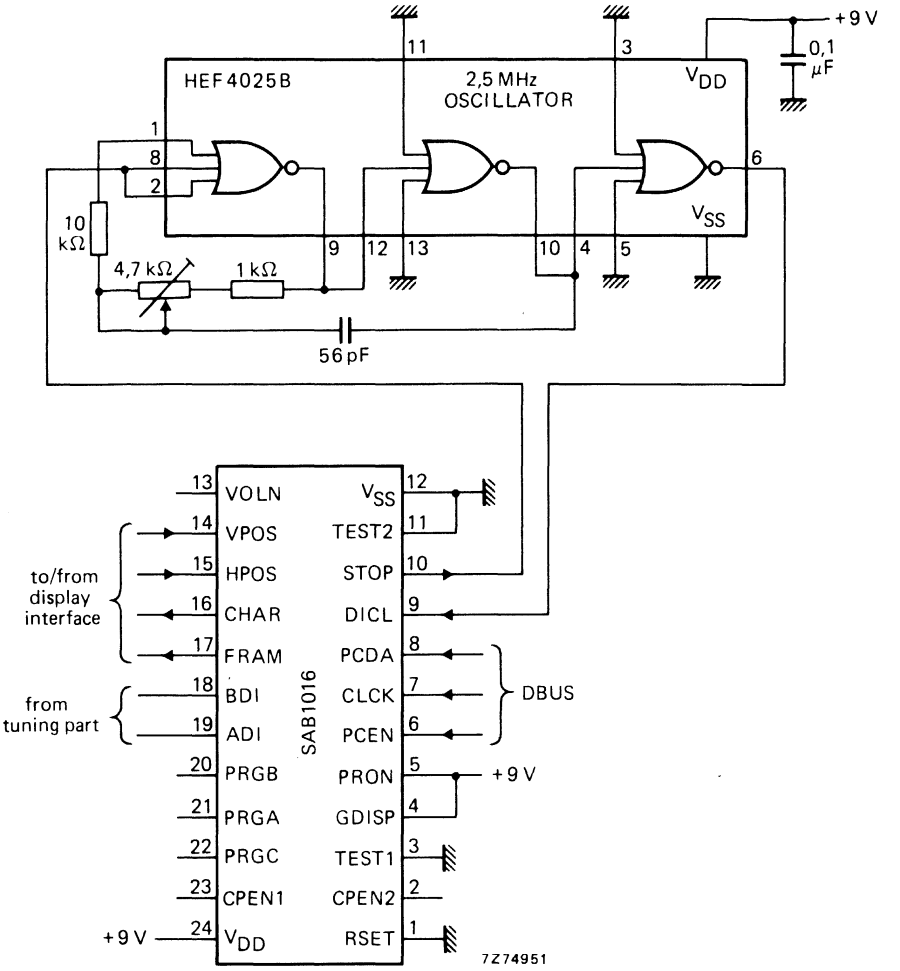


Fig. 10 Interconnection and display oscillator for SAB1016.

1 GHz DIVIDER-BY-256

This silicon monolithic integrated circuit is an ECL fixed-ratio divide-by-256 scaler for input frequencies in the range 70 to 1000 MHz, a supply voltage of 5 or 5,2 V and an ambient temperature of 0 to + 70 °C. The inputs of the circuit are differential and internally biased to permit capacitive coupling or asymmetrical drive. For a sinusoidal input waveform the device becomes insensitive at low frequencies due to edge rate limitations. Operation down to d.c. is possible with square-wave drive. The divide-by-256 outputs are designed to interface with C-MOS and N-MOS circuits having a common V_{EE} (ground). They provide active pull-up.

Pins marked n.c. should preferably be grounded. The circuit may oscillate in the absence of an input signal, but this oscillation is suppressed by the application of an input signal within the specified range.

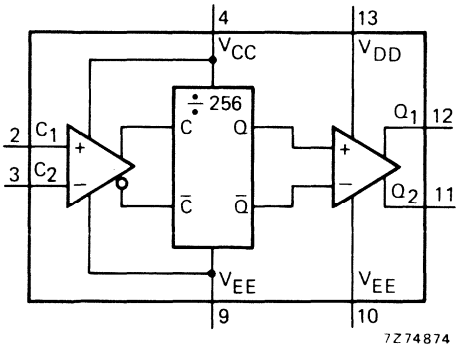


Fig. 1.

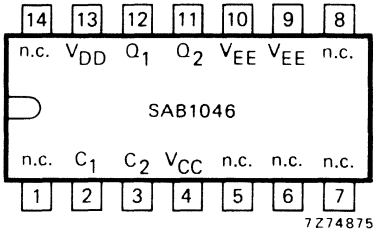


Fig. 2.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4,75 to 5,46 V
	V_{DD}		4,75 to 10 V
Input frequency range	f_i		70 to 1000 MHz
Q_1 (C-MOS) output voltage			
HIGH state	V_{OH}	min.	7,5 V
LOW state	V_{OL}	max.	1,5 V
Q_2 (N-MOS) output voltage			
HIGH state	V_{OH}	min.	2,4 V
LOW state	V_{OL}	max.	0,4 V
Power consumption per package (no load)	P_{av}	typ.	320 mW
Operating ambient temperature	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

SAB1046P: 14-lead DIL; plastic (SOT-27S, T, V).

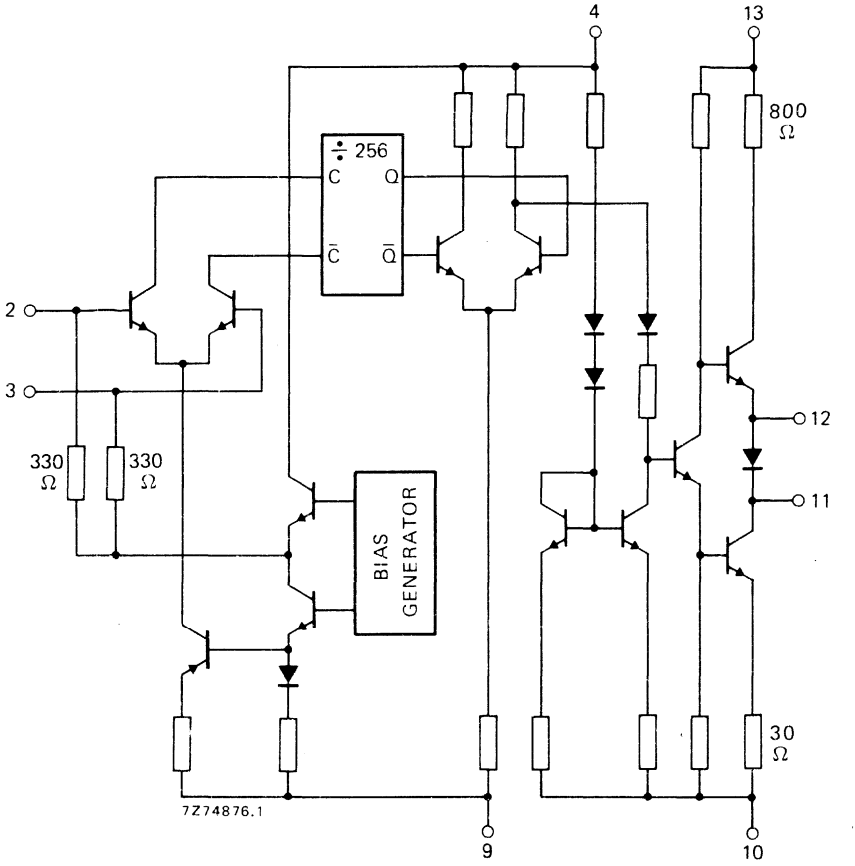


Fig. 3 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7 V
	V_{DD}	max.	10 V
Input voltage	V_I		0 to 5,2 V
Storage temperature	T_{stg}		−55 to + 125 °C
Junction temperature	T_j	max.	125 °C

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; V_{DD} = 9 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage Q_1 (pin 12); V_{DD} = 4,75 to 10 V			
HIGH: $I_{OH} = -1\ \mu A$	V_{OH}	$V_{DD}-1,5$ V to V_{DD}	V
LOW : $I_{OL} = 1\ \mu A$	V_{OL}	0 to 1,5	V
Output voltage Q_2 (pin 11); V_{DD} = 5 V			
HIGH: $V_{CC} = V_{DD} = 5$ V; $I_{OH} = -1\ \mu A$	V_{OH}	2,4 to 5	V
LOW : $V_{CC} = V_{DD} = 5$ V; $I_{OL} = 1\ \mu A$	V_{OL}	0 to 0,4	V
Reference voltage (pin 2 or 3)	V_{ref}	2,25 to 3	V
Supply current (pin 4) pin 2 = 0 V; pin 3 = open	I_{CC}	typ. 65	mA
		< 85	mA
Supply current (pin 13)	I_{DD}	typ. 3	mA
		< 5	mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 4,75 to 5,46 V; V_{DD} = 4,75 to 10 V; T_{amb} = 0 to 70 °C.

	symbol	pin under test	min.	typ.	max.		conditions
Input frequency	f_i		70	–	1000	MHz	sinusoidal input voltage $V_{i(p-p)}$ = 600 mV; * tested frequency on pin 11 or 12 is $f_i/256$
Differential input voltage	$\lvert V_2-V_3 \rvert_{p-p}$	2 and 3	–	–	1,4	V	
Slew rate for operation: down to 70 MHz			80	–	–	V/μs	square-wave drive $V_{i(p-p)}$ min. 160 mV *

Guaranteed operating region (see also Fig. 4)

		input frequency				
	MHz	70	200	500	900	1000
Minimum required input level $V_{i(p-p)}$ *	mV	355	160	140	100	200
	dBm	−5	−12	−13	−16	−10

* For definition of input voltage see Fig. 5.

A.C. CHARACTERISTICS (continued)

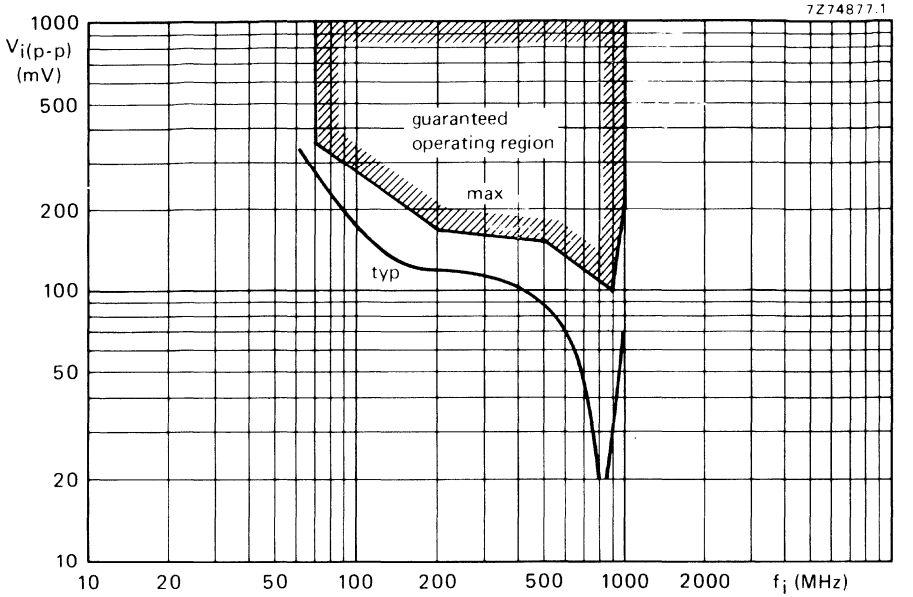


Fig. 4 V_{CC} = 5 V; V_{DD} = 5 to 9 V; T_{amb} = 0 to 70 °C.

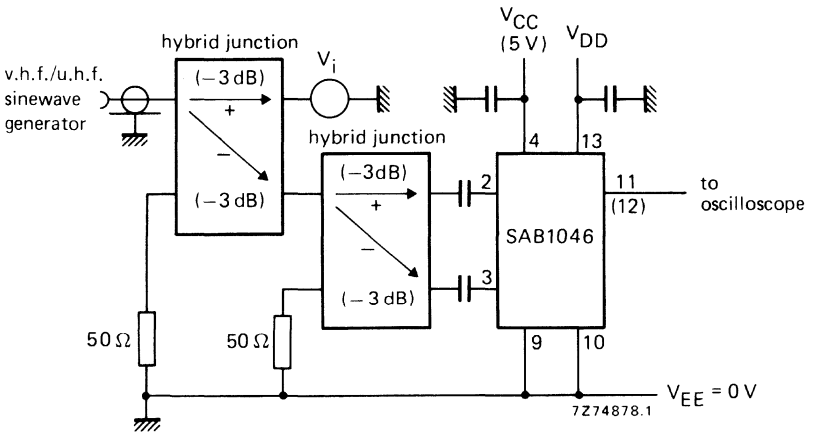


Fig. 5 Test circuit.

- Cable must be 50 Ω coaxial.
- The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
- All connections to the device must be kept short.
- Hybrid junctions are ANZAC H-183-4 or similar.

APPLICATION INFORMATION

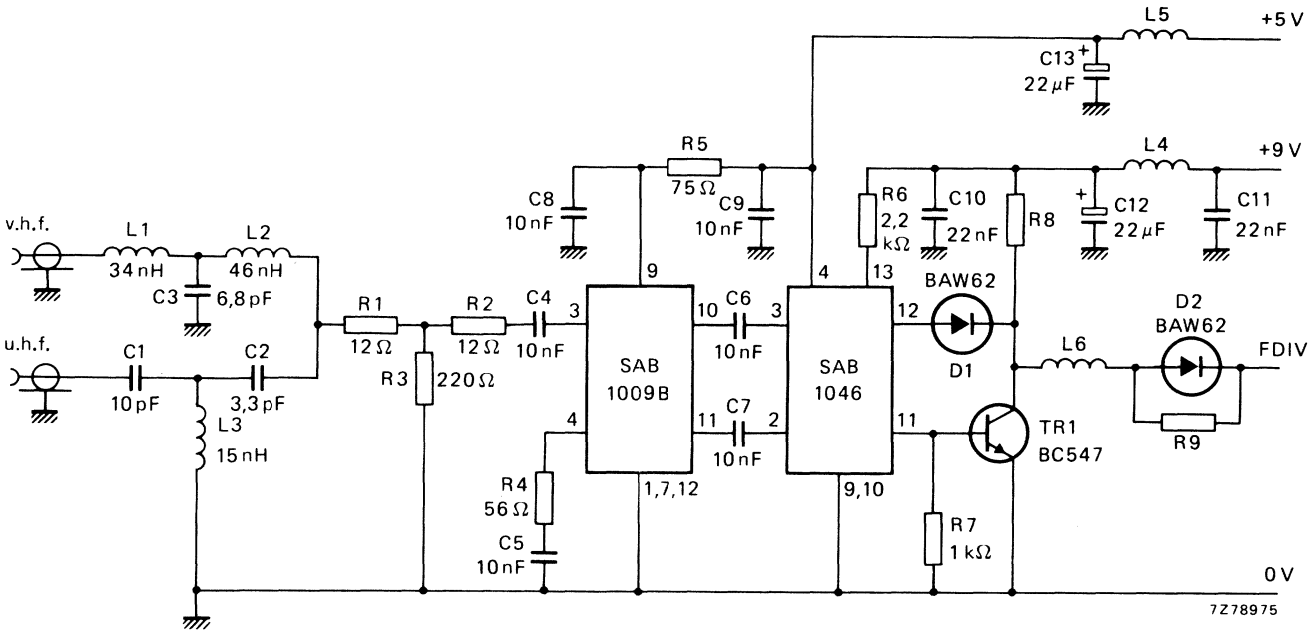


Fig. 6 H.F. divider for DICS in television receivers (prescaler module).

Values of R8, R9 and L6 have to be chosen in accordance with the load capacitance. The pins not mentioned are connected to ground except pin 5 of SAB1046 which is connected to V_{CC}.

APPLICATION INFORMATION (continued)

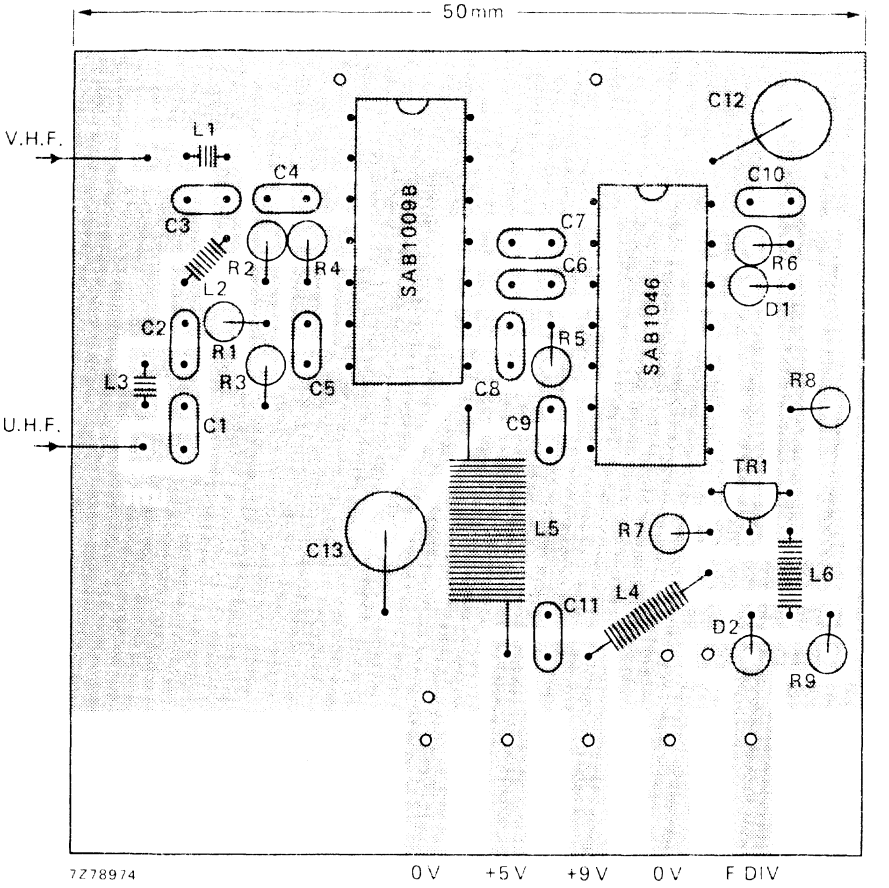


Fig. 7 Component layout of circuit shown in Fig. 6.

CONTROL AND STATION MEMORY CIRCUIT

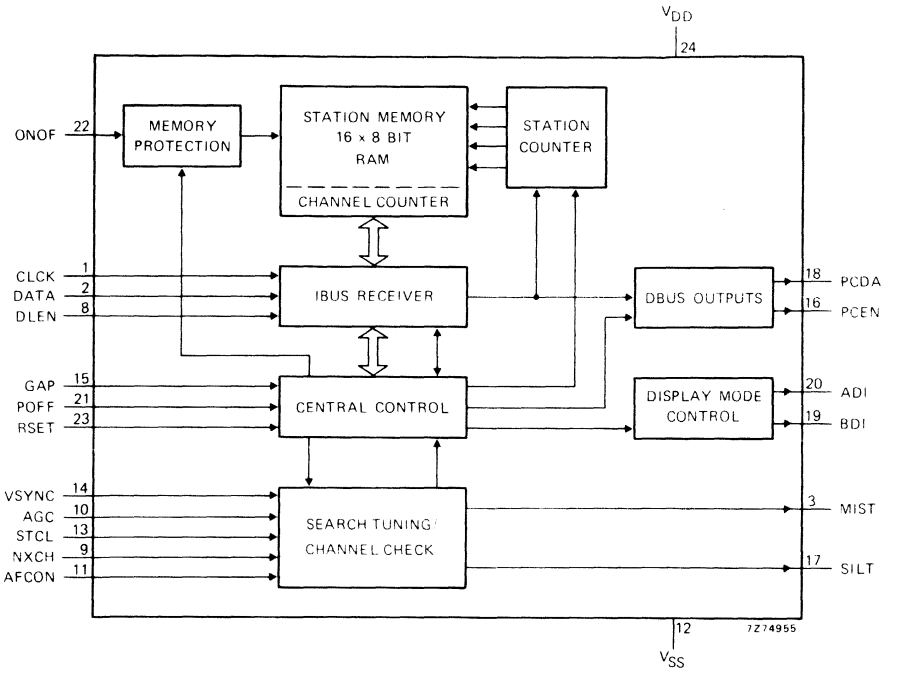


Fig. 1 Block diagram.

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	8 to 10	V
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Clock frequency	f_{CLCK}	typ. 62,5	kHz
Quiescent current; V_{DD} = 10 V; I_Q = 0; T_{amb} = 25 °C	I_{DD}	typ. 4	μA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The SAB2015 is the station memory and control circuit for the frequency control IC SAB2024. The device is implemented in LOCMOS, which requires only a small back-up battery to retain the station memory contents during power interruptions. The SAB2015 is driven and controlled via the serial data instruction bus (IBUS). The instructions applied via the IBUS control the following functions:

- The storage of up to 16 stations of the viewer's choice.
- Direct station selection.
- The bidirectional step station function.
- Direct channel number access.
- The bidirectional channel number step function.
- Bidirectional search tuning through all channels with automatic stop on location of a television transmission.
- The recall of last viewed station at POWER ON.
- Automatic muting in case of absence of transmission.

Information is transferred to the frequency control IC SAB2024 and the on-screen display IC SAB1016 via the DBUS station and/or channel select and display.

OPERATION DESCRIPTION

Data input

The SAB2015 can perform the instructions as listed in Table 1. The instructions are received in IBUS code; the instruction code, synchronized with the system clock, must be applied to input DATA. It will be accepted only if the data enable input DLEN is HIGH at the same time (for details see IBUS description).

Four modes of IBUS instructions are available:

- Station call instructions can modify only the station counter, the memory contents, and the channel counter.
- Channel mode instruction will only alter the contents of the channel counter.
- Recall instructions reproduce only the last DBUS output and can change the display mode control signals.
- The 'standby' instruction resets the system, while an unfinished instruction sequence will be aborted.

Table 1. IBUS instruction set

IBUS code no.	IBUS input code F	E	D	C	B	A	instruction mode
							station call instruction
16	0	1	0	0	0	0	16/on
17	0	1	0	0	0	1	1/on
18	0	1	0	0	1	0	2/on
19	0	1	0	0	1	1	3/on
20	0	1	0	1	0	0	4/on
21	0	1	0	1	0	1	5/on
22	0	1	0	1	1	0	6/on
23	0	1	0	1	1	1	7/on
24	0	1	1	0	0	0	8/on
25	0	1	1	0	0	1	9/on
26	0	1	1	0	1	0	10/on
27	0	1	1	0	1	1	11/on
28	0	1	1	1	0	0	12/on
29	0	1	1	1	0	1	13/on
30	0	1	1	1	1	0	14/on
31	0	1	1	1	1	1	15/on
36	1	0	0	1	0	0	step station up
37	1	0	0	1	0	1	step station down
							channel mode instruction; digit
16	0	1	0	0	0	0	0
17	0	1	0	0	0	1	1
18	0	1	0	0	1	0	2
19	0	1	0	0	1	1	3
20	0	1	0	1	0	0	4
21	0	1	0	1	0	1	5
22	0	1	0	1	1	0	6
23	0	1	0	1	1	1	7
24	0	1	1	0	0	0	8
25	0	1	1	0	0	1	9
34	1	0	0	0	1	0	set channel entry mode/on
5	0	0	0	1	0	1	search tuning up/on
35	1	0	0	0	1	1	search tuning down/on
38	1	0	0	1	1	0	step channel up/on
39	1	0	0	1	1	1	step channel down/on
							recall instruction
1	0	0	0	0	0	1	mute/on
4	0	0	0	1	0	0	display short; 2,5 seconds
32	1	0	0	0	0	0	display ON/OFF
33	1	0	0	0	0	1	store
							standby instruction
2	0	0	0	0	1	0	OFF

Data output

Each instruction running on the IBUS is checked for transmission errors by the on-chip IBUS receiver. Faultless received instructions are processed and start the output sequence to the DBUS, which contains 13 data bits in binary code and one leading zero bit (see Fig. 2 and Table 2).

1 leading zero bit
1 display mode bit
4 bits for station number
8 bits for channel number

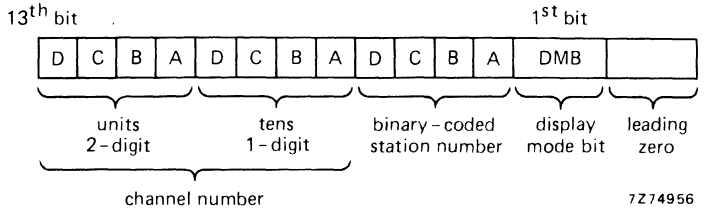


Fig. 2 DBUS instruction format.

The 1st bit of a DBUS instruction (DMB) is a display mode bit with the following code:

DMB	instruction
0	display of station and channel number
1	display of channel number only

Table 2. Specification of the DBUS code

DBUS input code D	C	B	A	channel number	station number
0	0	0	0	0	16
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	: *	10
1	0	1	1	blank *	11
1	1	0	0	blank *	12
1	1	0	1	blank *	13
1	1	1	0	blank *	14
1	1	1	1	blank *	15

* Not processed by the SAB2015.

DBUS transmission is synchronized with the system clock. A data enable signal is available at output PCEN in parallel with a data word at output PCDA (see Fig. 3). A DBUS sequence which possibly will be followed by a tuning operation is started after a delay of about 30 ms related to the end of a received instruction. The state of output SILT changes from LOW to HIGH directly after acceptance of an instruction, so click-free muting is achieved, even before the last selected transmitter is left.

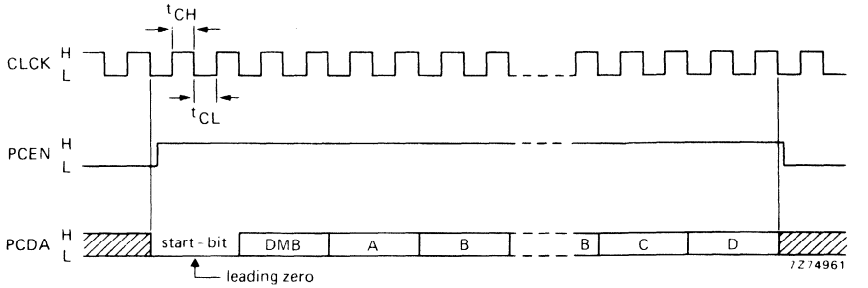


Fig. 3 Timing diagram for channel and station number information on DBUS.

PROCESSING OF INSTRUCTIONS

1. **Station/digit instructions**

Each station/digit instruction sets the display mode bit (DMB) in the DBUS transmission LOW (except in case 1.1.3c)

1.1. Set station number (1 to 16)

The processing of these IBUS instructions depends on the preceding instructions.

1.1.1. The corresponding digit will be stored in the station counter, if the instructions 'set channel entry mode' or 'store' were not previously received. The channel number stored under that address is read from the memory.

DBUS transmission:

DMB = LOW	+	station number	+	stored channel number

1.1.2. Instruction 'store' previously given; two kinds of operation are possible:

a. Last instruction before the 'store' instruction was a 'channel mode' instruction. The station number is then taken from the station counter and the channel counter contents are stored under the new address in the RAM.

DBUS transmission:

DMB = LOW	+	station number	+	channel number from channel counter

b. Last instruction before the 'store' instruction was a 'station' instruction. The channel number which was stored under the 'old' station number is then restored in the RAM under the new address or new station number.

DBUS transmission:

DMB = LOW	+	station number	+	stored channel number

1.1.3. Instruction 'set channel entry mode' previously given; three kinds of operation are possible:

a. The instruction contains a digit which is greater than 9; the instruction is then not processed, nor will there by any DBUS transmission.

b. The IBUS station/digit instruction, which is transferred, contains the first digit (0 to 9) of a channel number.

DBUS transmission:

DMB = HIGH	+	blank	+	1st digit + blank

c. One digit has already been entered. The channel selection sequence is completed after the second station/digit instruction and is transferred to the channel counter. This results in the output of the channel number at the DBUS.

DBUS transmission:

DMB = HIGH	+	station number	+	channel number from channel counter

1.2. Step station (up /down)

The contents of the station counter are incremented or decremented by 1. The channel number stored under the new address is read from the memory.

DBUS transmission:

DMB = LOW	+	station number ± 1	+	stored channel number

2. **Channel mode instructions**

Each channel instruction sets the display mode bit of the DBUS transmission to HIGH.

2.1. Set channel entry mode/on

This instruction prepares the system for a direct entry of two digits for a two-digit channel number.

DBUS transmission:

DMB = HIGH	+	3 blanks

2.2. Step channel (up/down)

The execution of these instructions depends on the kind of the last preceding instruction.

a. The step channel instruction follows a station instruction. The channel number stored under the preceding station number is incremented or decremented by 1, as long as there is no identifying signal for unallocated channel numbers at input GAP (see note 1). The new channel number is stored in the channel counter.

DBUS transmission:

DMB = HIGH	+	station number	+	stored channel number ± 1

b. The step channel instruction follows a channel instruction. The contents of the channel counter are incremented or decremented by 1, as long as there is no identifying signal for unallocated channel numbers at input GAP (see note 1).

DBUS transmission:

DMB = HIGH	+	station number	+	channel number from channel counter ± 1

Note 1. Identification of unallocated channel numbers

The numbers in the series 00 to 99 are not all allocated in the CCIR standard TV channels, so it is meaningless to step through channels which have no TV channel allocated. The frequency control IC SAB2024 therefore produces at its output GAP a HIGH signal for channel numbers 00, 01, 13 to 20 and 70 to 99 for as long as the circuit is not driven by an enable signal for special and cable TV channels. The HIGH signal is applied to input GAP of SAB2015 and causes rapid increment or decrement of the channel number, until GAP is set LOW.

2.3. Search tuning (up/down)

These IBUS instructions initialize an automatic step channel operation starting at the last selected channel (up or down) with one step to start with. Further stepping will happen if the NXCH input is drawn HIGH. This is the case if the frequency control IC SAB2024 has run through a micro-step tuning range and with the HIGH signal at its NXCH output demands that the next channel number is given to the DBUS.

Due to the identification of unallocated channels at a HIGH signal at input GAP, a tuning process in these ranges is suppressed also in case of search tuning.

DBUS transmission at NXCH = HIGH:

DMB = HIGH	+	station number	+	channel number from channel counter ± 1

Search tuning stops automatically if a received transmission is suitable for viewing. A running search operation can be stopped by the instructions:

station call
set channel entry mode/on
step station (up/down)
step channel (up/down)
OFF

3. **Recall instruction**

All these instructions lead to the repetition of the last preceding station or channel DBUS transmission.

4. **Standby instruction**

The 'OFF' instruction resets the following signal processing circuit parts to the standby state:

search tuning
store
display (2,5 s)
set channel entry mode

The 'OFF' instruction starts no DBUS transmission.

5. **Display mode control outputs** (ADI and BDI)

The state of the mode control signals ADI and BDI is determined by the input conditions shown in Table 3.

Table 3.

input POFF	received IBUS instructions					outputs	
	search tuning (running)	store	set channel	on-screen display (2,5 s)	on-screen display ON/OFF	ADI	BDI
1	X	X	X	X	X	0	0
0	1	X	X	X	X	1	1
0	0	1	0	X	X	0	0
0	X	X	1	X	X	0	1
0	0	0	0	0	1	0	1
0	0	0	0	1	0	1	0

0 = IBUS instruction should not be received previously.
1 = IBUS instruction received.
X = eventually previously received IBUS instruction will be reset.

6. **Television transmission identification; muting signal**

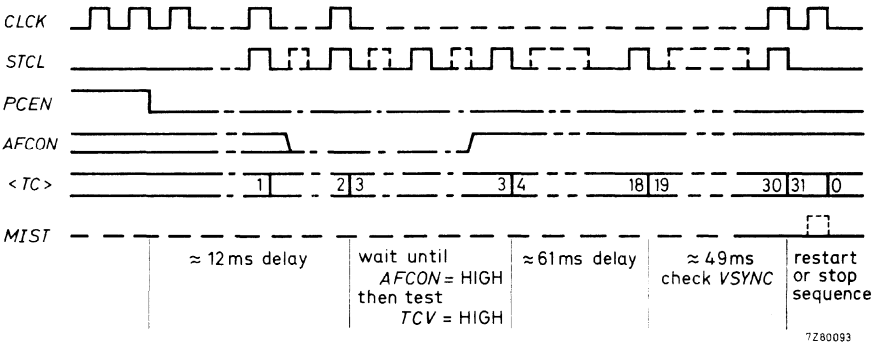
In order to determine if a received transmission is suitable for viewing, particular timing requirements of the input signals AFCON, AGC and VSYNC must be fulfilled (see Fig. 4). The automatic channel-check will be started in 2 cases:

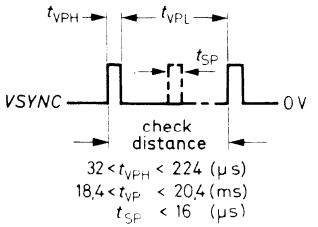
a. By an instruction which starts a new tuning procedure.
b. When the automatic frequency control is switched off (AFCON = LOW).

For as long as the channel-check circuit has not recognized a suitable transmitter, the circuit produces a muting signal (SILT = HIGH). The channel-check is finished, i.e. a transmitter is recognized as suitable, if the following criteria are fulfilled:

a. Digital tuning must be finished, i.e. automatic frequency control is on (AFCON = HIGH).
b. The tuner control voltage is switched on (AGC = HIGH).
c. Correct video sync pulses are present (VSYNC = HIGH).

If one of these criteria fails, then output MIST generates a micro-step pulse for switching over to the next micro-step range and channel-check starts the next cycle.





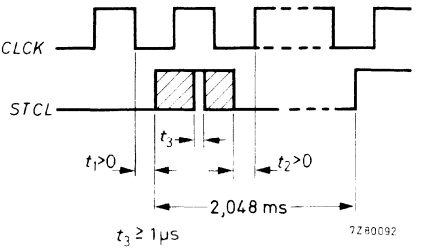


Fig. 4 Simplified channel-check timing diagrams.

7. **Memory protection circuit**

Switching off of the system supply voltage can be recognized at input POFF. A LOW to HIGH transition of this input signal is interpreted as the beginning of a power-off operation. Therefore all circuit outputs are forced LOW at the next HIGH to LOW transition of the system clock and no further operation can be started until the POFF signal returns to LOW. If, however, the processing of an instruction has been initialized immediately before the LOW to HIGH transition of the POFF signal, then this operation (and the DBUS transmission) is finished before the power-off signal is accepted. In this case a maximum of 32 clock pulses are necessary.

After a HIGH to LOW transition of POFF, a DBUS transmission 'display short; 2,5 seconds' is automatically generated for starting the frequency control IC SAB2024.

The SAB2015 needs a back-up battery for memory retention.

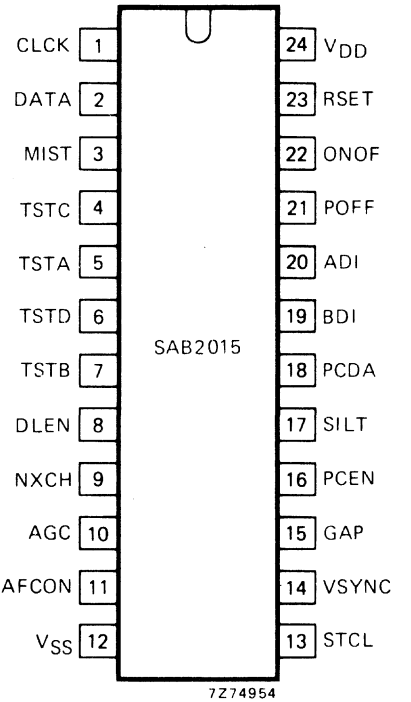


Fig. 5 Pinning diagram.

PINNING

24	V_{DD}	positive supply
12	V_{SS}	negative supply (0 V)

Inputs

1	CLCK	system clock; 62,5 kHz
2	DATA	IBUS data signals
8	DLEN	IBUS data line enable signals
9	NXCH	a HIGH at the input selects the next channel during search tuning
10	AGC	automatic gain control; tuner voltage control
11	AFCON	automatic frequency control; HIGH = AFC on
13	STCL	search tuning clock; repetition rate 2,048 ms
14	VSYNC	vertical sync input
15	GAP	identifying signal for unallocated channel numbers
21	POFF	memory protection signal
22	ONOF	memory enable signal; a LOW inhibits the write operation
23	RSET	reset signal; a HIGH at the input completely resets the circuit except for the station memory
5	TSTA	test inputs
7	TSTB	

Outputs

3	MIST	control signal for incrementing the micro-step tuning counter
16	PCEN	DBUS data enable signal
17	SILT	muting signal during tuning
18	PCDA	DBUS data signal
19	BDI	display mode control outputs
20	ADI	
4	TSTC	test outputs
6	TSTD	

RATINGS (V_{SS} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

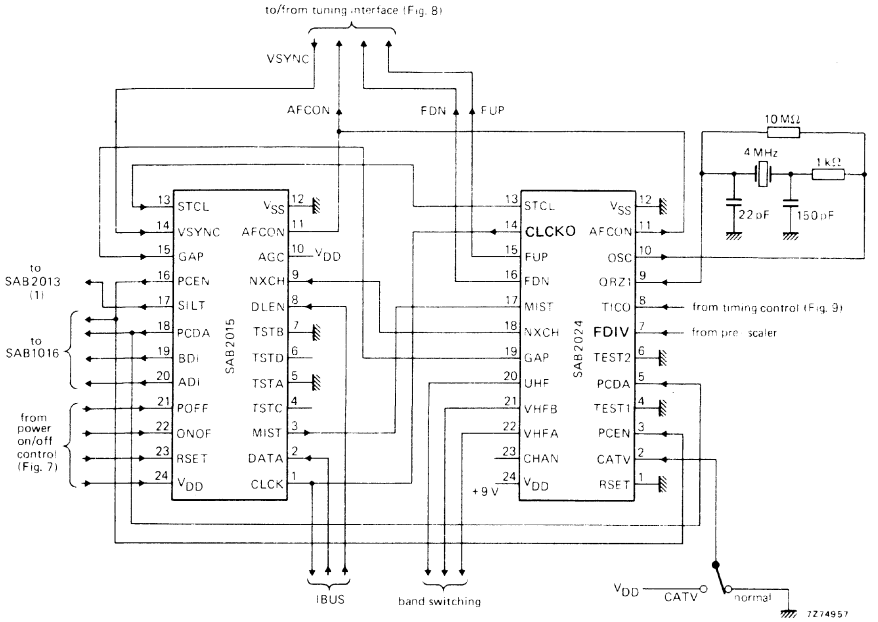
Supply voltage range	V_{DD}		−0,3 to + 11	V
Input voltage range	V_I		−0,3 to + V_{DD} + 0,3	V
Input current	$\pm I_I$	max.	10	mA
Output current	$\pm I_O$	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	300	mW
Operating ambient temperature range	T_{amb}		0 to + 70	°C
Storage temperature range	T_{stg}		−55 to + 150	°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; unless otherwise specified

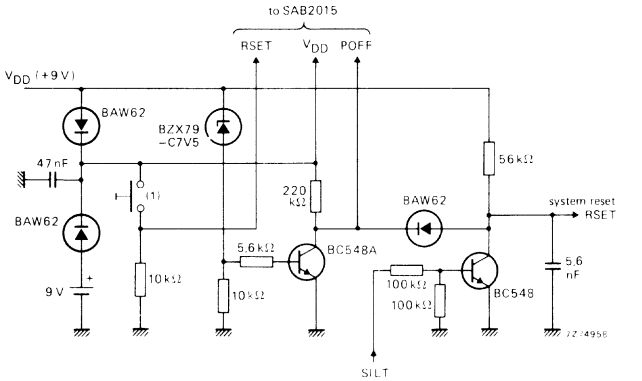
	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	8	9	10	V	
Quiescent current per package	10	I_{DD}	–	–	20	μA	I_O = 0; T_{amb} = 25 °C; inputs to V_{DD} or V_{SS}
Input leakage current	8 to 10	I_{IR}	–	–	1	μA	T_{amb} = 25 °C; inputs 10 V
		$-I_{IR}$	–	–	1	μA	T_{amb} = 25 °C; inputs V_{SS}
Input voltage LOW	8 to 10	V_{IL}	0	–	1,5	V	
Input voltage HIGH	8 to 10	V_{IH}	V_{DD}−1,5	–	V_{DD}	V	
Output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_O = 1 mA
Output voltage HIGH	8 to 10	V_{OH}	V_{DD}−1	–	–	V	$-I_O$ = 1 mA
Outputs TSTC; TSTD							
Output voltage LOW	8 to 10	V_{OL}	–	–	0,1	V	I_O = 0,1 mA
Output voltage HIGH	8 to 10	V_{OH}	V_{DD}−2	–	–	V	$-I_O$ = 0,5 mA
Clock frequency	8 to 10	f_{CLCK}	0	62,5	100	kHz	
Duty factor	8 to 10	δ	0,2	–	0,8		
Input rise/fall time	8 to 10	t_r; t_f	–	–	1	μs	

Supply voltage transition rate: dV_{DD}/dt = 0,1 V/μs.



(1) Output SILT can be used for muting during channel mode operations and/or dark tuning.

Fig. 6 Interconnection diagram of the SAB2015 and SAB2024 used in a tuner circuit.



(1) Operate button to clear station memory of SAB2015 after battery charge. System reset pulse RSET will remain LOW if tuning operation is in progress.

Fig. 7 Power ON/OFF circuitry; used in combination with Fig. 6.

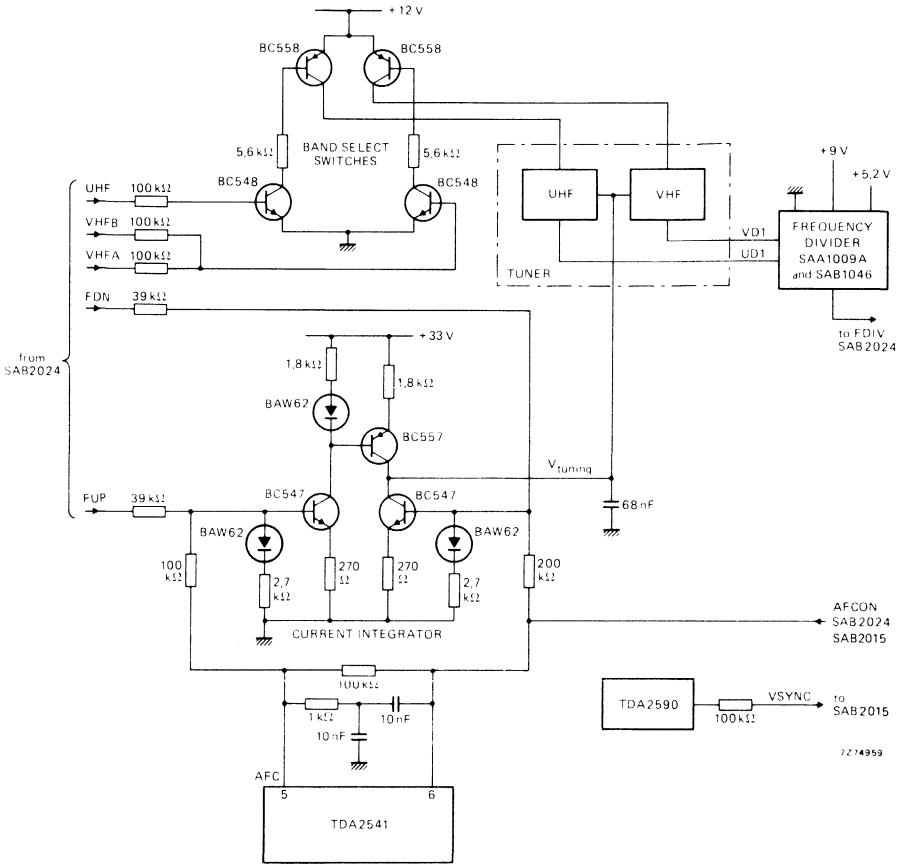
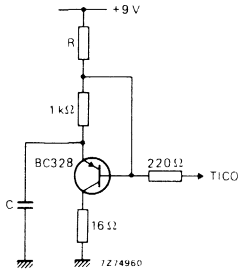


Fig. 8 Tuning interface and band select; used in combination with Fig. 6.



R_{max} = 470 kΩ

C_{max} = 560 nF

$t_{v\,max}$ = 130 ms

$t_{v\,max}$ is the maximum delay which can be obtained under worst-case conditions.

Fig. 9 Tuning constants at input TICO (Fig. 6).

INSTRUCTION ENCODER

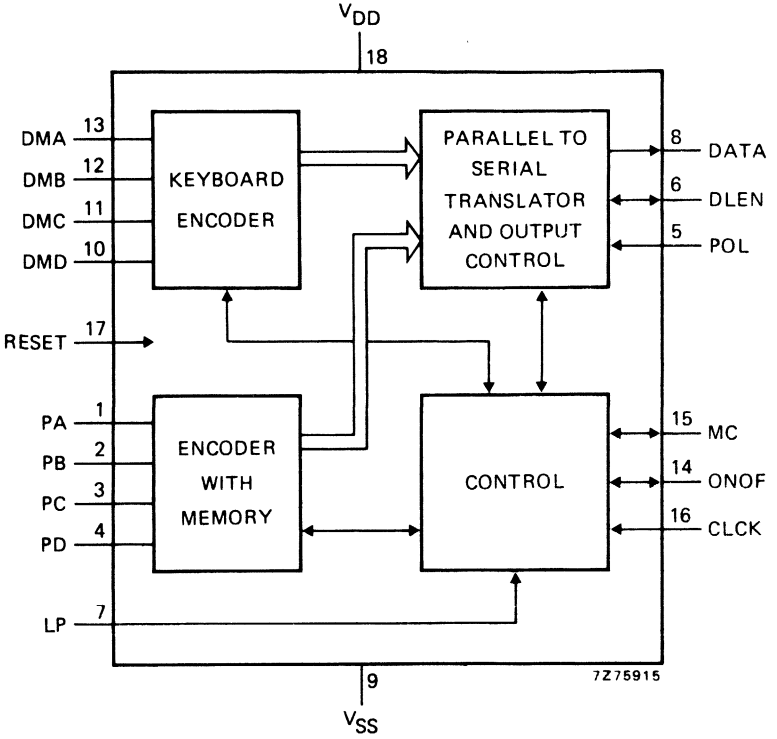


Fig. 1 Block diagram.

Features

- Parallel to serial keyboard encoder; used in the DICS (Digital Channel Select) system with the SAB2015 and SAB2024.
- Parallel/serial conversion of 4-bit parallel information for station/channel selection in the tuning system.
- External time constant for generating a delay time for key bouncing.
- Serial instruction output; compatible with the DICS IBUS interface.

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,75 to 10	V
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Clock frequency	f_{CLCK}	typ. 62,5	kHz
Quiescent current; V_{DD} = 10 V; I_Q = 0; T_{amb} = 25 °C	I_{DD}	typ. 20	μA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

GENERAL DESCRIPTION

The SAB2021 is intended as a control circuit with parallel input for the serial instruction bus (IBUS) of the DICS system (as shown in Fig. 2). The circuit can be used for local control of the tuning system. The possibilities of the parallel inputs allow connection of remote control systems with parallel output of instructions.
The device is implemented in LOCMOS technology.

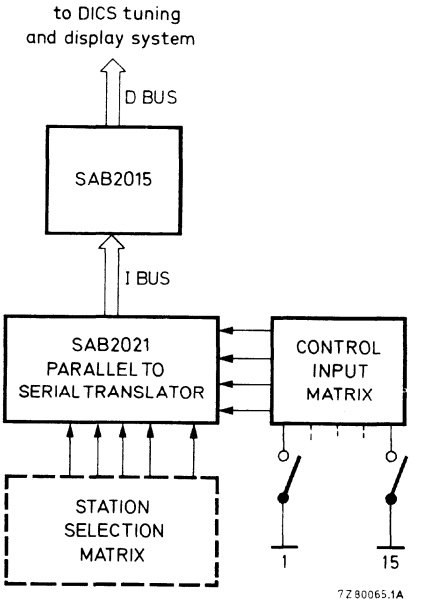


Fig. 2 Circuit SAB2021 providing local control.

OPERATION DESCRIPTION

Station/channel select inputs (PA, PB, PC, PD and LP)

A parallel instruction at inputs PA to PD generates the serial output of an IBUS data word. A data word contains a coded digit instruction for 1 to 16/0, and is used in the tuning system (SAB2015) for station call or direct channel selection.

Truth table 1. Station call instruction

inputs					output	IBUS code	IBUS instruction code						instruction (SAB2015)	
LP	PA	PB	PC	PD	ONOF	no.	F	E	D	C	B	A	station number	channel number
0	1	1	1	1	0	16	0	1	0	0	0	0	0/16	0
0	0	0	0	0	0	17	0	1	0	0	0	1	1	1
0	1	0	0	0	0	18	0	1	0	0	1	0	2	2
0	0	1	0	0	0	19	0	1	0	0	1	1	3	3
0	1	1	0	0	0	20	0	1	0	1	0	0	4	4
0	0	0	1	0	0	21	0	1	0	1	0	1	5	5
0	1	0	1	0	0	22	0	1	0	1	1	0	6	6
0	0	1	1	0	0	23	0	1	0	1	1	1	7	7
0	1	1	1	0	0	24	0	1	1	0	0	0	8	8
0	0	0	0	1	0	25	0	1	1	0	0	1	9	9
0	1	0	0	1	0	26	0	1	1	0	1	0	10	
0	0	1	0	1	0	27	0	1	1	0	1	1	11	
0	1	1	0	1	0	28	0	1	1	1	0	0	12	
0	0	0	1	1	0	29	0	1	1	1	0	1	13	
0	1	0	1	1	0	30	0	1	1	1	1	0	14	
0	0	1	1	1	0	31	0	1	1	1	1	1	15	
1	X	X	X	X	X	–	no output operation							

An IBUS data output can be initialized in 2 ways:

a. An output is initialized by an H/L transition at input LP (Fig. 3). The data word contains the coded instruction at the inputs PA to PD. Station selection and direct channel selection in the tuning system are possible in this mode. The inputs DMA to DMD overrule the LP signal.

b. When LP = LOW: the data word output is initialized by new information at the inputs (Fig. 4). Only station selection is possible in this mode of operation.

Only one IBUS data word is generated in both cases.

DEVELOPMENT SAMPLE DATA

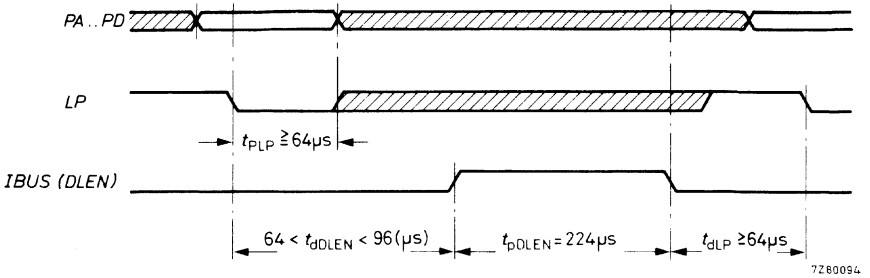


Fig. 3 Output operation initialized by LP (load station); f_{CLCK} = 62,5 kHz.

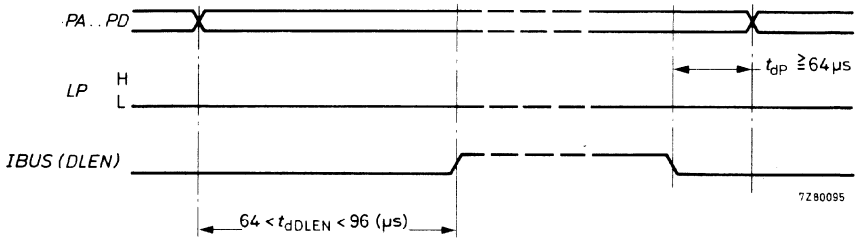


Fig. 4 Output operation initialized by new information at inputs PA to PD; f_{CLCK} = 62,5 kHz.

Tuning control inputs (DMA, DMB, DMC, DMD)

A parallel instruction at the input DMA to DMD generates one of 15 IBUS instructions for controlling the tuning system. The arrangement is shown in truth table 2.

An IBUS data word is initialized if one or more of these inputs are switched from the quiescent state HIGH to LOW. An output is only possible out of the quiescent state HIGH. A key operation at the inputs must last until the IBUS data transmission is finished. If the key contact is opened before an output operation was initialized no output appears (Fig. 5).

The instruction via DMA to DMD is ineffective if an output operation, initialized via the inputs PA to PD and LP is in progress. If the bus-line is occupied (DLEN = HIGH) the output is delayed until the bus is free, and then carried out for as long as initialization is still present (Fig. 6).

Truth table 2. Tuning control instructions

inputs				IBUS instruction code						output	IBUS code	instruction for SAB2015
DMA	DMB	DMC	DMD	F	E	D	C	B	A	ONOF	nr.	
1	0	1	1	0	0	0	1	0	1	0	5	search tuning up
1	1	1	0	1	0	0	0	0	1	–	33	store
0	1	1	1	1	0	0	0	0	0	–	32	display on/off
0	1	0	1	1	0	0	1	1	0	0	38	step channel up
1	1	0	1	1	0	0	0	1	0	0	34	channel mode
0	0	1	1	0	0	0	1	0	0	0	4	display mode (2,5 s)
1	1	0	0	1	0	0	0	1	1	0	35	search tuning down
1	0	0	1	1	0	0	1	1	1	0	39	step channel down
0	0	0	1	1	0	0	1	0	0	0	36	step station up
1	0	0	0	1	0	0	1	0	1	0	37	step station down
0	1	0	0	0	0	0	0	1	0	1	2	off
0	0	1	0	1	1	0	0	0	0	–	48	fine detuning up*
0	1	1	0	1	1	0	0	0	1	–	49	fine detuning down*
1	0	1	0	1	1	0	0	1	0	–	50	fine detuning basic*
0	0	0	0	1	1	0	1	1	0	0	54	decimal 1*
1	1	1	1	no output operation						–	–	no key information

* Not applicable for the SAB2015, but for SAB2022.

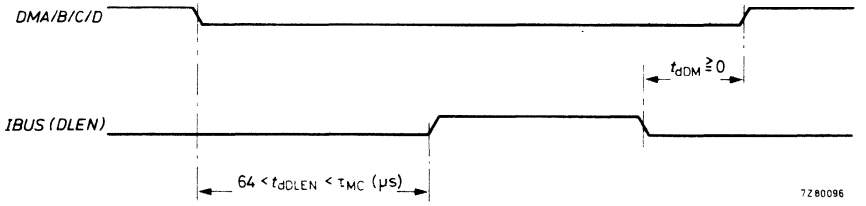


Fig. 5 Output operation initialized by a LOW state at DMA to DMD; f_{CLCK} = 62,5 kHz.

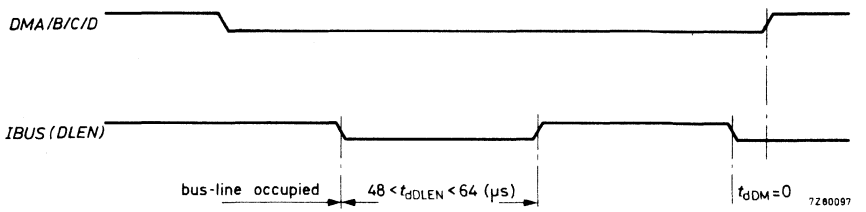


Fig. 6 Output operation after release of the bus-line DLEN; f_{CLCK} = 62,5 kHz.

DEVELOPMENT SAMPLE DATA

Clear input (RESET)

A HIGH at the input completely resets the circuit.

Polarization input (POL)

This output controls the polarity of the outputs DLEN and DATA.

input POL	output	
HIGH	DATA	DLEN
LOW	$\overline{\text{DATA}}$	$\overline{\text{DLEN}}$

Input/output (MC)

The terminal MC is the output of a p-channel driver stage in conjunction with a Schmitt trigger input. An RC network at the input generates a delay of the output operation after the inputs DMA to DMD are activated. The delay time should overlap the key bounce time.

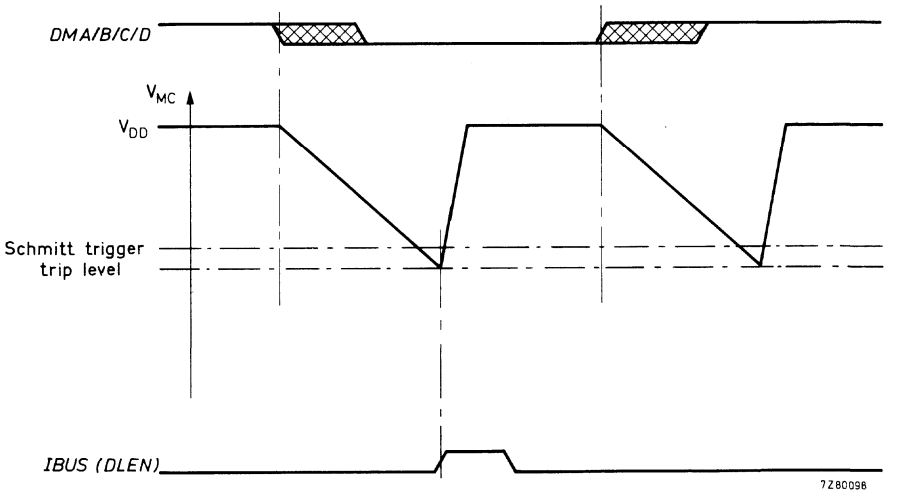


Fig. 7 Overlap of key bouncing by a delay time at input/output MC.

Input/output (ONOF)

The terminal ONOF is the output of a flip-flop. It can be switched to the LOW = ON state by a series of instructions (see Tables 1 and 2). The instruction 'off' sets the output in the stand-by state, ONOF = HIGH. A HIGH at RESET also sets the output in the stand-by state. The 'ON' state can also be attained by forcing the ONOF output to LOW for at least 2 clock periods of the clock frequency.

System clock input (CLCK)

The 62,5 kHz system clock is connected to this input.

IBUS outputs (DATA, DLEN)

The circuit generates the serial data words necessary for driving and controlling the tuning system (SAB2015).
The data transmission is initialized by:
a. Keyboard instructions at inputs PA to PD, if LP = LOW.
b. An H/L transition at input LP.
c. Keyboard instructions at inputs DMA to DMD.

The IBUS data word has a length of 6-bits + 1 start-bit; the data line enable (DLEN) signal is sent for control purposes (Fig. 8).

Input/output (DLEN)

The data line enable output (DLEN) is HIGH during output operation (POL = HIGH).
In the non-operation mode the DLEN terminal operates as an input for recognition of the bus-line occupied. For this purpose, the terminal is connected to V_{SS} (POL = HIGH) or to V_{DD} (POL = LOW) via a resistor.

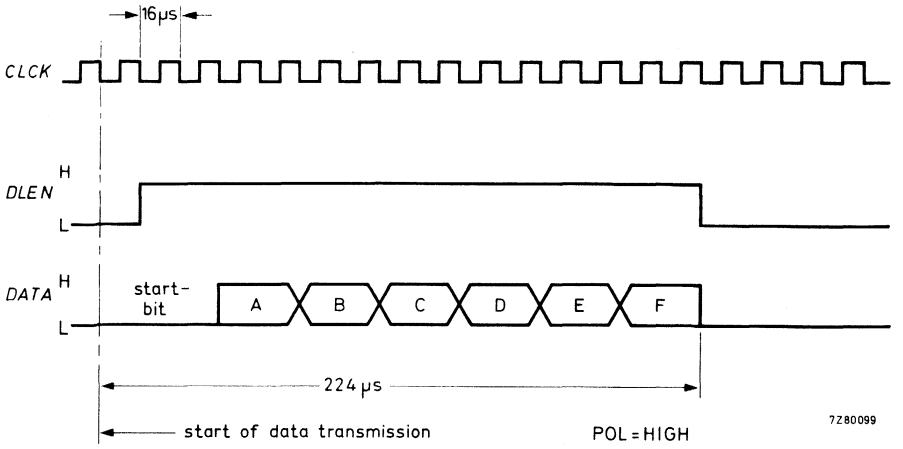


Fig. 8 Timing diagram of the IBUS data transmission (DLEN and DATA).

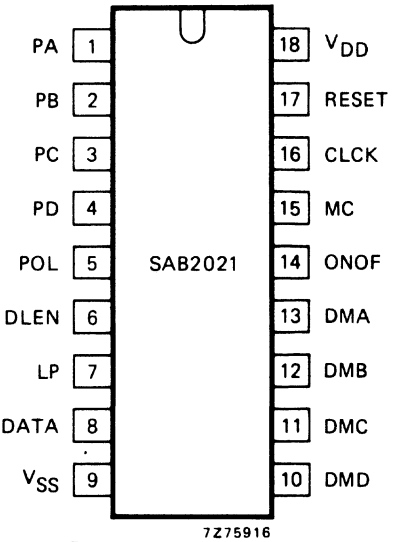


Fig. 9 Pinning diagram.

PIINING

18	V_{DD}	positive supply
9	V_{SS}	negative supply (0 V)

Inputs

1	PA	station/channel select inputs
2	PB	
3	PC	
4	PD	
7	LP	load station
17	RESET	clear input
13	DMA	tuning control inputs
12	DMB	
11	DMC	
10	DMD	
16	CLCK	system clock
5	POL	polarization input

Inputs/outputs

14	ONOF	'stand-by' input/output
15	MC	debouncing terminal
6	DLEN	data line enable input

Output

8	DATA	IBUS data output

RATINGS (V_{SS} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 11	V
Input voltage range	V_I	−0,3 to + V_{DD}	V
Input current	$\pm I_I$	max. 10	mA
Output current	$\pm I_O$	max. 10	mA
Power dissipation per output	P_O	max. 50	mW
Total power dissipation per package	P_{tot}	max. 300	mW
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	4,75	9	10	V	
Quiescent current	10	I_{DD}	–	–	50	μA	I_O = 0; inputs V_{SS} or V_{DD}
Input leakage current	10	I_{IR}	–	–	1	μA	inputs 10 V; T_{amb} = 25 °C
		$-I_{IR}$	–	–	1	μA	inputs V_{SS}; T_{amb} = 25 °C
Input voltage LOW	4,75 to 10	V_{IL}	0	–	0,3 V_{DD}	V	
Input voltage HIGH	4,75 to 10	V_{IH}	0,7 V_{DD}	–	V_{DD}	V	
Outputs DATA, DLEN, ONOF, MC 3-state outputs							
Output impedance	4,75 to 10	R_{FLT}	100	–	–	kΩ	non-conducting mode
Output voltage HIGH	4,75 to 10	V_{OH}	V_{DD}−0,8	–	–	V	$-I_O$ = 0,4 mA
Output voltage LOW	4,75 to 10	V_{OL}	–	–	0,8	V	I_O = 0,4 mA
Schmitt-trigger inputs MC, LP							
Trip level HIGH	4,75	V_{IHT}	3,3	–	–	V	
	10	V_{IHT}	7,0	–	–	V	
Trip level LOW	4,75	V_{ILT}	–	–	1,4	V	
	10	V_{ILT}	–	–	3,0	V	
Clock frequency	4,75 to 10	f_{CLCK}	0	62,5	100	kHz	
Input rise/fall time	4,75 to 10	t_r; t_f	–	–	1	μs	
	4,75 to 10	t_r; t_f	–	–	10	μs	all inputs except MC, LP

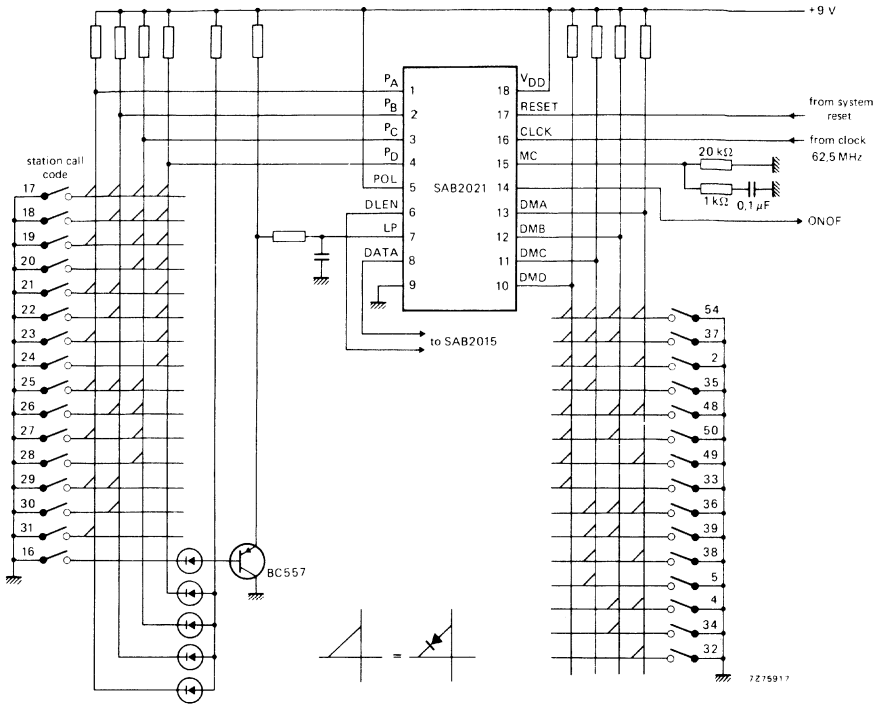


Fig. 10 Interconnection diagram SAB2021 used for local control.

FINE DETUNING CIRCUIT

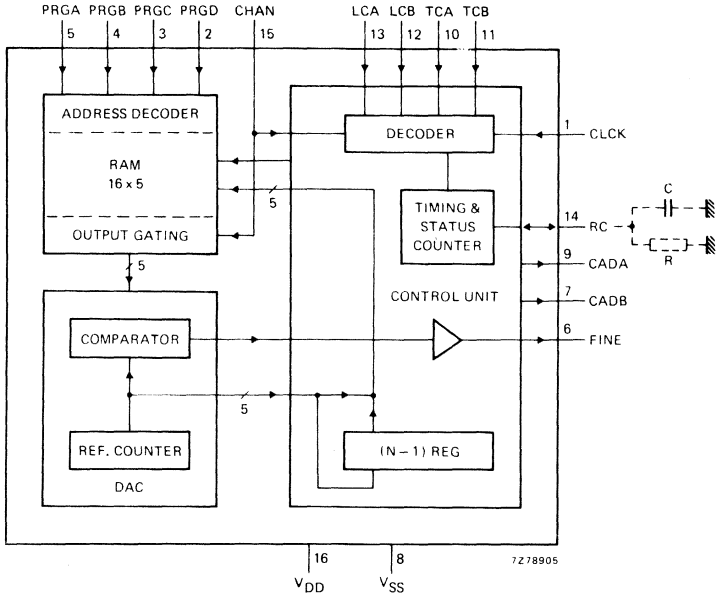


Fig. 1 Block diagram.

Features

- 16 analogue settings can be stored.
- Control input for basic setting.
- Single or automatic bidirectional increments.
- Externally adjustable stepping speed.
- Extremely small quiescent current consumption.
- Memory protection circuit incorporated.

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	8 to 10	V
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Clock frequency	f_{CLCK}	typ. 62,5	kHz
Quiescent current; V_{DD} = 10 V; I_Q = 0; T_{amb} = 25 °C	I_{DD}	< 20	μA

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

GENERAL DESCRIPTION

The SAB2022 is an optional integrated circuit of the DICS system (Digital Channel Select). It stores the fine detuning offsets for 16 pre-selected stations in 31 steps. The device is implemented in LOCMOS technology and needs a back-up battery to retain the memory contents.

The IC has a 16 x 5-bit read/write memory (RAM) for storing the binary-coded analogue values, a digital/analogue converter and a control unit. It operates as a 16-fold analogue memory with serial access. Each analogue value is selected by a 4-bit address at the address inputs PRGA, PRGB, PRGC and PRGD. The addressed 5-bit word is converted into a pulse-width modulated signal and is available at output FINE. The conversion is completed with a simple external integration network. An analogue setting can be changed by a LOW signal at the key inputs TCA and/or TCB. An external RC time constant omits key-bounce problems and also determines the stepping speed.

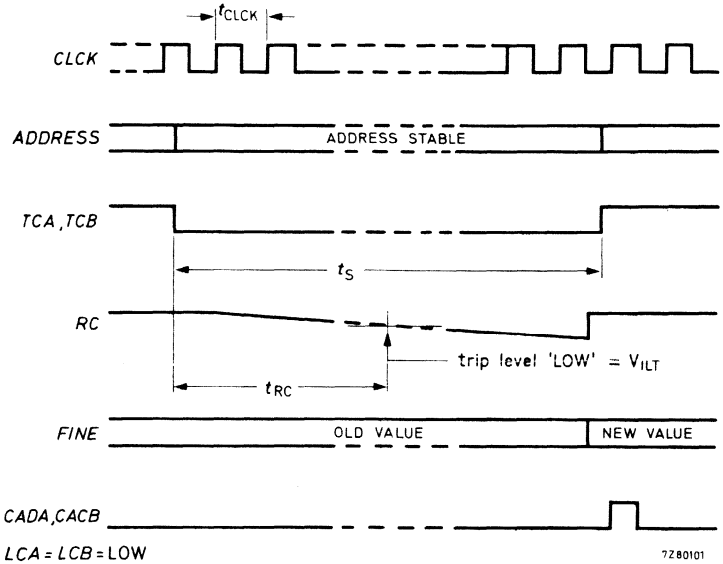
A basic value of about 50% of the analogue value can be generated for each address, independent of the stored analogue value.

The mode of operation is controlled by two inputs (LCA, LCB); e.g. the stand-by mode, in which all outputs are LOW, the keyboard inputs are disabled, and the memory content is retained by means of a 3,3 V supply.

OPERATION DESCRIPTION

Address inputs (PRGA, PRGB, PRGC, PRGD)

The binary coded address (e.g. station information) applied to these inputs selects one of the sixteen 5-bit words with the corresponding analogue values, if the circuit operates in the normal mode (LCA = LCB = LOW) and input CHAN is LOW.
The content of the addressed memory (initiated at CHAN) is then available at output FINE. The stored value can be changed by the key control inputs TCA and TCB; the address signals must be stable during that time.



$$384\,t_{CLCK} + t_{RC} \leq t_S \leq 1664\,t_{CLCK} + 4t_{RC} \quad (\text{for } t_{RC} > 0)$$

$$t_{RC} = RC \ln \frac{V_{ILT}}{V_{DD}}$$

Fig. 2 Single step change of a stored analogue value.

Key control inputs (TCA, TCB)

The inputs are coded instruction keyboard inputs and the addressed information can be changed via both inputs. The inputs are effective, if the device is in the normal mode and input CHAN is LOW. The inputs operate by the following codes:

inputs		function
TCA	TCB	
1	1	start position
0	1	step function down; decrease of analogue output value
1	0	step function up; increase of analogue output value
0	0	basic value; 50% of analogue value

The instructions are accepted only after a delay time t_{RC}, in order to avoid erroneous information caused by key bouncing. The delay time is determined by an external RC circuit at terminal RC. Each instruction, which is applied during the time t_S (see Fig. 2), leads to a change in the memory contents and thus of the analogue value by 1 step. If the instruction is applied for a longer period (continuous operation) then there will only be a further change in the analogue value after a time t_A (see Fig. 3); i.e. after a period of about 4 x t_{RC}. Thus in continuous operation, automatic stepwise changes can be achieved.

Basic set input (CHAN)

A HIGH level applied to this input generates the 50% analogue level (basic set) independently of addressing at output FINE. The key control inputs TCA and TCB are inhibited. The CHAN signal is effective during normal operation (LCA = LCB = LOW).

Mode control inputs (LCA, LCB)

The mode of operation is determined by the signals at inputs LCA and LCB.

inputs		operation mode
LCA	LCB	
1	1	test
0	1	reset all internal flip-flops
1	0	stand-by (all outputs LOW)
0	0	normal

Time constant input/output (RC)

This terminal is an input of an internal Schmitt-trigger as well as an output for an external RC time constant (open drain, p-channel). An external capacitor and resistor in parallel (see Fig. 1) determine a delay time for key bouncing suppression.
If TCA and TCB are HIGH, then the RC circuit will be continuously charged (start position). The charging will be interrupted by a key instruction and discharging starts. Discharging is detected by the trip level 'LOW' of the internal Schmitt-trigger and defines the end of the delay time. If automatic step function is applied, RC will be charged with a pulse corresponding to 128 system clock periods in duration (see Fig. 3).

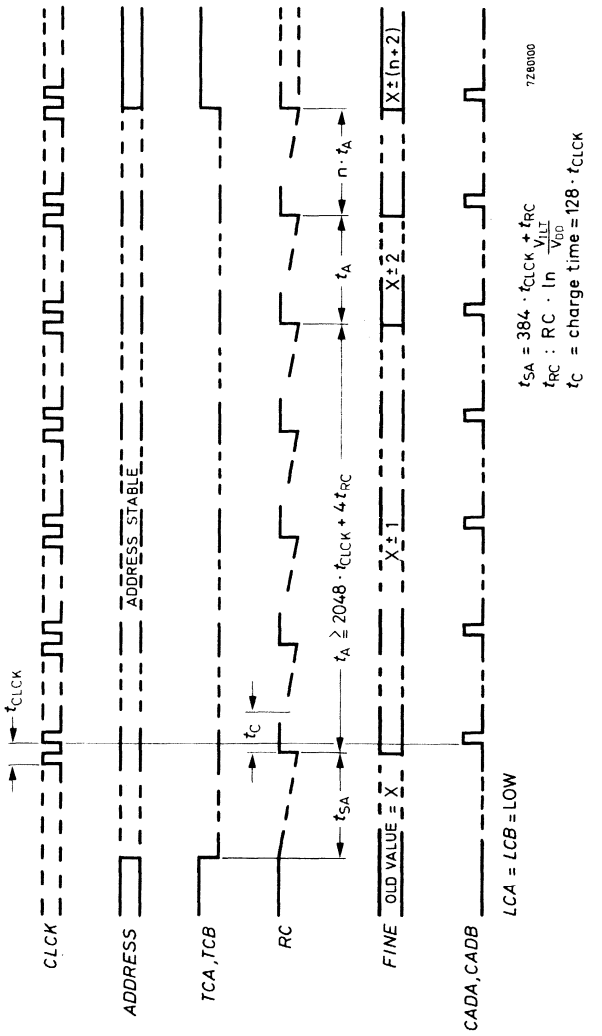


Fig. 3 Automatic step function.

Analogue output (FINE)

The 5-bit word stored in the read/write memory (RAM) is converted into a pulse-width modulated signal and is available at output FINE. The signal is a pulse train with a repetition rate of 32 x 4 = 128 clock periods. Variation of 32 steps are possible.

step 1 : final value; smallest analogue setting; reached by step function down; output duty factor = 1/32.

step 15: basic value (50%); attained when TCA = TCB = LOW or CHAN = HIGH or by step function; duty factor = ½.

step 32: final value; largest analogue setting; reached by step function up; duty factor = 1 (HIGH output signal).

The analogue voltage corresponding to the pulse code at the analogue output is obtained by using simple integrating networks.

Control outputs (CADA, CADB)

The control signals CADA and CADB present additional information, e.g. control of display and/or for remote drive of the SAB2022. When an instruction on TCA or TCB is applied the corresponding output (CADA, CADB) generates a single pulse per step. The pulse will be repeated with a time interval t_{RC} of the external time constant, because automatic step function is used (see truth table below and Fig. 4). If a final value is reached the corresponding output generates an output signal of ¼ x f_{CLCK} with a duty factor of 0,5.
As long as TCA = TCB = LOW and output FINE generates the basic value or if CHAN = HIGH, a frequency of 1/128 x f_{CLCK} appears at both outputs CADA and CADB.

Truth table

inputs			outputs		operation mode
TCA	TCB	CHAN	CADA	CADB	
0	1	0	P1	0	decrease of analogue output value
1	0	0	0	P1	increase of analogue output value
0	0	0	P1	P1	basic value; 50% of analogue value
X	X	1	P2	P2	basic value; 50% of analogue value
X	1	0	P3	0	final value; step 1
1	X	0	0	P3	final value; step 32

X = state is immaterial
P1, P2 and P3: see Fig. 4.

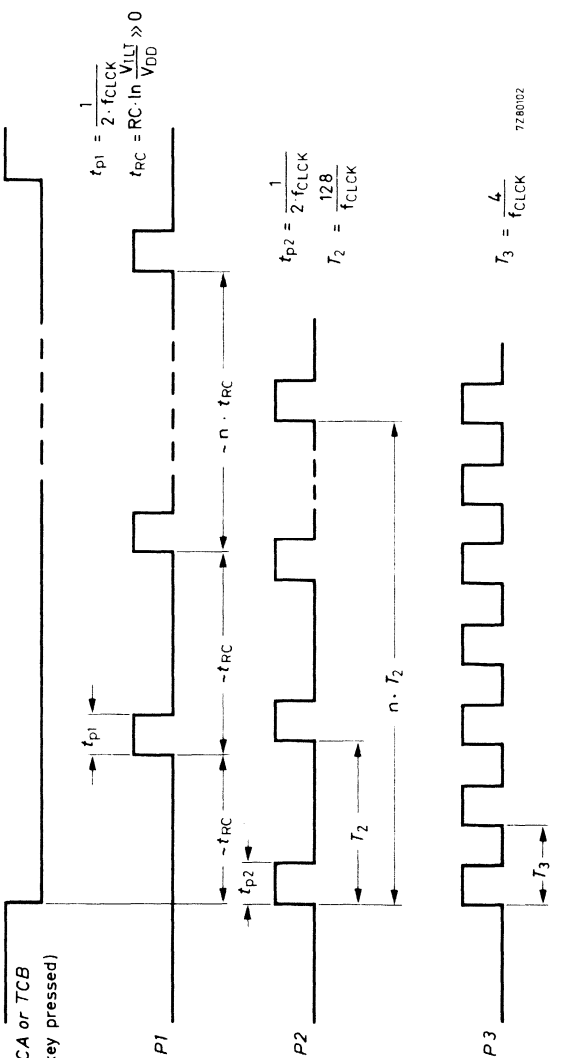


Fig. 4 Waveforms showing interrelationship between inputs TCA, TCB and outputs P1, P2 and P3 at CADA or CADB; see also truth table.

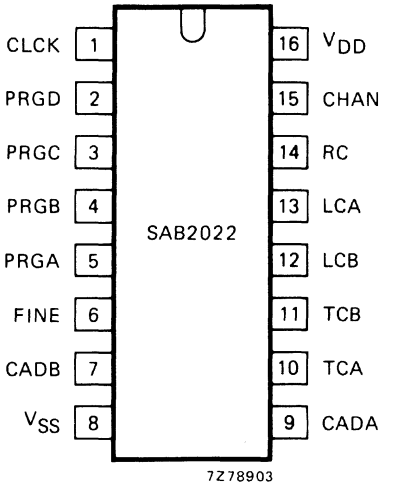


Fig. 5 Pinning diagram.

PINNING

Inputs

1	CLCK	system clock; 62,5 kHz
2	PRGD	address inputs (station inputs)
3	PRGC	
4	PRGB	
5	PRGA	
10	TCA	key control inputs
11	TCB	
12	LCB	mode control inputs
13	LCA	
15	CHAN	basic set input

Input/output

14	RC	time constant output; Schmitt-trigger input

Outputs

6	FINE	analogue output
7	CADB	control outputs
9	CADA	

RATINGS (V_{SS} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 11		V
Input voltage range	V_I	−0,3 to + V_{DD}		V
Input current	$\pm I_I$	max.	10	mA
Output current	$\pm I_O$	max.	10	mA
Power dissipation for outputs FINE, RC	P_O	max.	100	mW
Power dissipation for outputs CADA, CADB	P_O	max.	50	mW
Total power dissipation per package	P_{tot}	max.	300	mW
Operating ambient temperature range	T_{amb}	0 to + 70		°C
Storage temperature range	T_{stg}	−55 to + 150		°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	8	9	10	V	
Supply voltage for retention data at stand-by	–	V_{DDR}	3,3	–	–	V	
Supply current for retention data at stand-by	–	I_{DDR}	–	–	20	μA	all inputs V_{SS} or V_{DD}; T_{amb} = 25 °C; I_Q = 0
Supply voltage transition rate	–	dV_{DD}/dt	–	–	0,1	V/μs	
Input leakage current	10	I_{IR}	–	–	1	μA	T_{amb} = 25 °C; inputs 10 V
		$-I_{IR}$	–	–	1	μA	T_{amb} = 25 °C; inputs V_{SS}
Input voltage LOW	8 to 10	V_{ISL}	0	–	1,5	V	
Input voltage HIGH	8 to 10	V_{ISH}	V_{DD}−1,5	–	V_{DD}	V	
Schmitt-trigger input RC							
Trip level HIGH	8	V_{IHT}	5,6	–	–	V	
	10	V_{IHT}	7,0	–	–	V	
Trip level LOW	8	V_{ILT}	–	–	2,4	V	
	10	V_{ILT}	–	–	3,0	V	

CHARACTERISTICS (continued)

V_{SS} = 0; T_{amb} = 0 to + 70 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Outputs CADA; CADB; FINE							
Output voltage HIGH	8 to 10	V_{QH}	$V_{DD}-1$	–	–	V	$-I_{QH}$ = 1 mA
Output voltage LOW	8 to 10	V_{QL}	–	–	1	V	I_{QL} = 1 mA
Output RC							
Output voltage HIGH	8 to 10	V_{QH}	$V_{DD}-1$	–	–	V	p-channel on; $-I_{QH}$ = 1 mA
Output leakage current	10	I_{QR}	–	–	10	μA	p-channel off
Clock frequency	8 to 10	f_{CLCK}	0	62,5	100	kHz	
Input rise/fall time	8 to 10	t_r; t_f	–	–	1	μs	

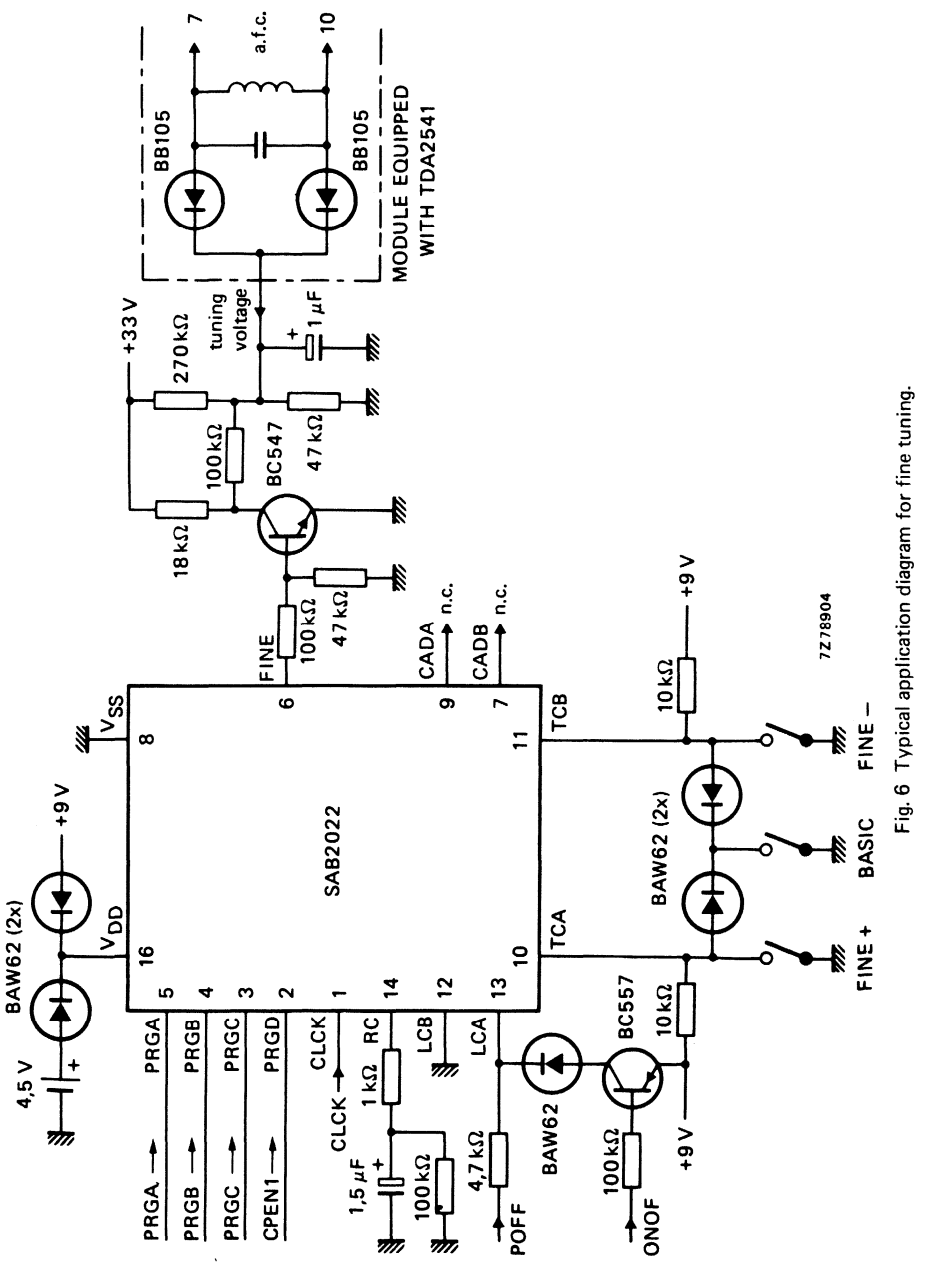


Fig. 6 Typical application diagram for fine tuning.

FREQUENCY CONTROL CIRCUIT

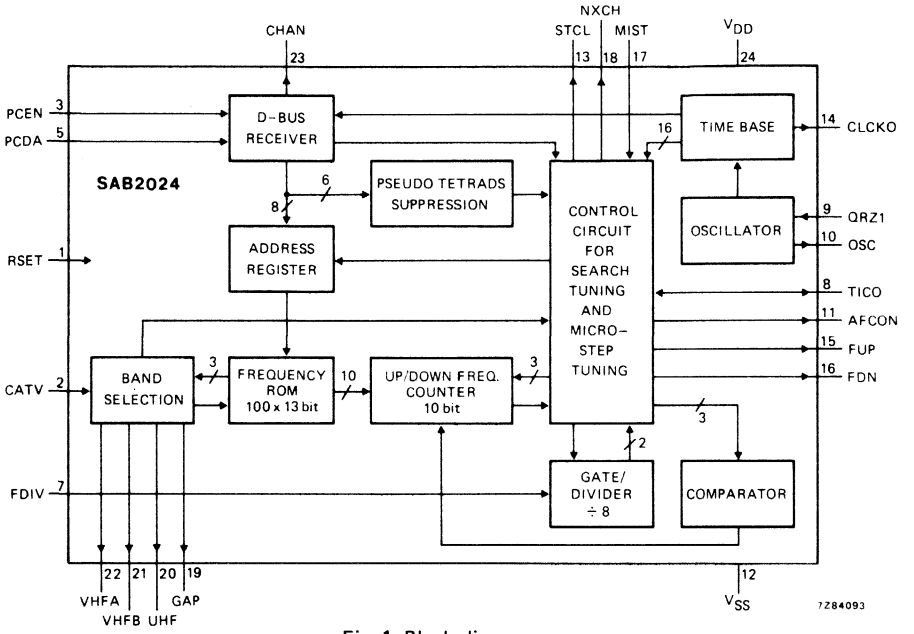


Fig. 1 Block diagram.

Features

- Automatic band switching, determined by the channel numbers.
- Micro-step tuning for unallocated frequencies.
- Control signal for AFC on/off.
- CATV channels available.
- Improved selection in respect of adjacent channels.

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	8 to 10 V
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Oscillator input frequency	f_{QRZ1}	< 4,5 MHz
Frequency divider input frequency range	f_{FDIV}	0,3 to 3,5 MHz
Quiescent current; V_{DD} = 10 V; I_Q = 0; T_{amb} = 25 °C	I_{DD}	typ. 40 μA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The frequency control circuit SAB2024 measures continuously the oscillator frequency of the TV tuner. Together with the prescaler and the tuner it forms the frequency locked-loop in the DICS system (Digital Channel Selection). When a tuning procedure is started, the oscillator frequency of the TV tuner is measured and corrected until the deviation in frequency found is within the specified limit. After that the automatic frequency control (AFC) part of the TV set is switched on to complete the tuning.

Frequency measurement

The actual measurement is done within a fixed time of 2048 μs, which is derived from the 4 MHz crystal oscillator. Before the measurement starts, the frequency counter is loaded with the addressed contents from the frequency ROM. This content is the binary equivalent of the desired oscillator frequency of the tuner in MHz. The frequency counter is now decremented with the incoming frequency applied at input FDIV within the 2048 μs. Any remaining frequency in the frequency counter at the end of the measuring time generates a pulse to outputs FUP or FDN with a duration proportional to the tuning error. This pulse is used to modify the tuning voltage. By means of this, the oscillator returns to the desired frequency within the range −337,5 kHz to + 787,5 kHz. When the digital tuning is complete, the offset inaccuracy is set to −1337,5 kHz to + 787,5 kHz. The AFC is then switched on to complete the tuning operation.

ROM program

As already mentioned, the ROM is programmed with the binary coded local oscillator frequencies (x + 39) MHz, calculated from

$$f_{osc} = f_{carrier} + \text{i.f.} = (x{,}25 + 38{,}9)\ \text{MHz},$$

associated with 100 (00 to 99) channels as shown in Tables 1 and 2.

Channels 77 to 99 are reserved for the S-band, used in CATV systems. The unused channels are automatically bypassed, indicated by signal GAP being HIGH. The ROM also generates the required band switch information as given in Tables 1 and 3. An adaption to Italian channels is possible (with the SAB2034).

Micro-step tuning

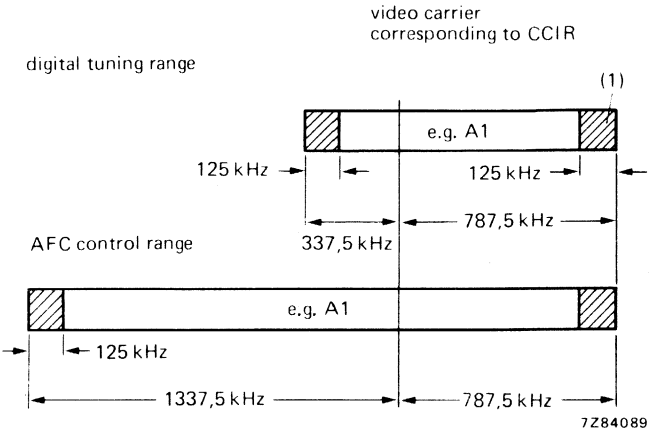
To enable the location of transmission of unallocated frequencies, the DICS system incorporates the micro-step tuning facility. Whenever a channel is selected and the TV transmission is not present, the micro-step tuning will automatically come into operation (see Fig. 3). The local oscillator frequency is detuned in five discrete steps away from the centre frequency in such a way that a complete coverage of the entire band is obtained.
If a station is not detected, the micro-step will be automatically continued, except for search tuning. In that case a channel step will be done.
Whenever a TV carrier drifts in frequency and comes outside the AFC control range (see Fig. 2), the micro-step tuning is restarted, thus within the channel range, the system follows the TV carrier.

Band switching and band ends

During band switching or during micro-step tuning, the system can tune to frequency areas outside the specified band ends. This results in an out of order situation for the control loop. A time constant is generated to avoid unwanted system blocks. If the tuner does not deliver the desired frequency in a time t_d (see Fig. 7) the output AFCON pulse will be set HIGH and the normal transmitter identification will be started. The delay time t_d is externally controlled by an RC network connected to input TICO. This delay time must be long enough, for the system to tune properly and reliably under all conditions (see Fig. 12).

Data bus instruction format

The format and timing of the DBUS is shown in Figs 4 and 5. Only the channel number information is relevant to the SAB2024, namely, the channel number addresses the frequency ROM.



(1) Possible error in frequency measurement.

Fig. 2 Digital tuning and control range.

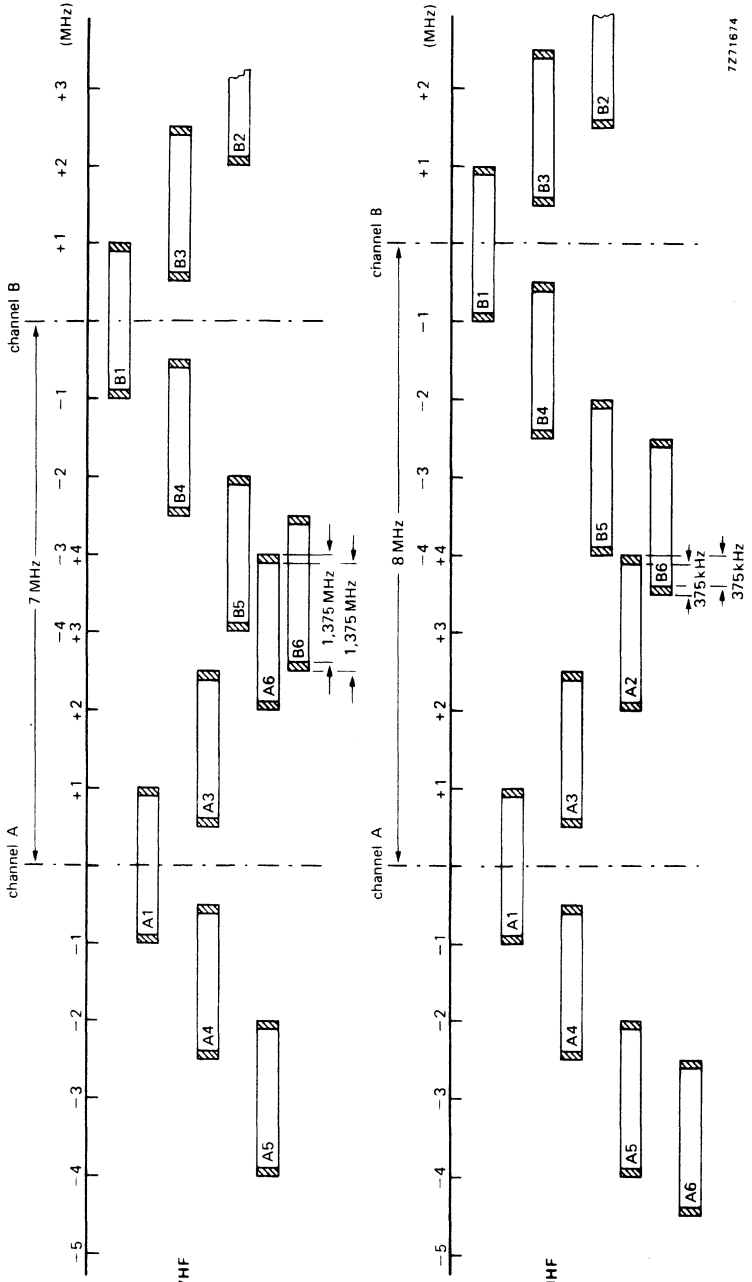


Fig. 3 Micro-step tuning. The shaded 125 kHz areas are maximum tuning errors.

Table 1. DICS channel numbers and allocated TV channels (VHF).

channel designation			CATV = 0		CATV = 1		
DICS channel number	special channels	European channels	VHF A	VHF B	VHF A	VHF B	frequency range
2		E2					47 MHz
3		E3					
4		E4					68 MHz
77	S1						
78	S2						
79	S3						89 MHz
							104 MHz
80	M1						
81	M2						
82	M3						
83	M4						
84	M5						
85	M6						
86	M7						
87	M8						
88	M9						
89	M10						
							174 MHz
5		E5					
6		E6					
7		E7					
8		E8					
9		E9					
10		E10					
11		E11					
12		E12					
							230 MHz
90	U1						
91	U2						
92	U3						
93	U4						
94	U5						
95	U6						
96	U7						
97	U8						
98	U9						
99	U10						
							300 MHz

Table 2. DICS channel number (ROM addresses) and the allocated frequencies (VHF and UHF).

address DICS channel number	video carrier freq. MHz	f_{osc} ROM contents MHz	address DICS channel number	video carrier freq. MHz	f_{osc} ROM contents MHz	address DICS channel number	video carrier freq. MHz	f_{osc} ROM contents MHz
00	44,25	83	34	575,25	614	67	839,25	878
01	44,25	83	35	583,25	622	68	847,25	886
02	48,25	87	36	591,25	630	69	855,25	894
03	55,25	94	37	599,25	638	70	44,25	83
04	62,25	101	38	607,25	646	71	44,25	83
05	175,25	214	39	615,25	654	72	44,25	83
06	182,25	221	40	623,25	662	73	44,25	83
07	189,25	228	41	631,25	670	74	44,25	83
08	196,25	235	42	639,25	678	75	44,25	83
09	203,25	242	43	647,25	686	76	44,25	83
10	210,25	249	44	655,25	694	77	69,25	108
11	217,25	256	45	663,25	702	78	76,25	115
12	224,25	263	46	671,25	710	79	83,25	122
13	44,25	83	47	679,25	718	80	105,25	144
14	44,25	83	48	687,25	726	81	112,25	151
15	44,25	83	49	695,25	734	82	119,25	158
16	44,25	83	50	703,25	742	83	126,25	165
17	44,25	83	51	711,25	750	84	133,25	172
18	44,25	83	52	719,25	758	85	140,25	179
19	44,25	83	53	727,25	766	86	147,25	186
20	44,25	83	54	735,25	774	87	154,25	193
21	471,25	510	55	743,25	782	88	161,25	200
22	479,25	518	56	751,25	790	89	168,25	207
23	487,25	526	57	759,25	798	90	231,25	270
24	495,25	534	58	767,25	806	91	238,25	277
25	503,25	542	59	775,25	814	92	245,25	284
26	511,25	550	60	783,25	822	93	252,25	291
27	519,25	558	61	791,25	830	94	259,25	298
28	527,25	566	62	799,25	838	95	266,25	305
29	535,25	574	63	807,25	846	96	273,25	312
30	543,25	582	64	815,25	854	97	280,25	319
31	551,25	590	65	823,25	862	98	287,25	326
32	559,25	598	66	831,25	870	99	294,25	333
33	567,25	606						

Note: ROM content is $f_{osc} = f_{carrier} + i.f. = x,25 + 38,9 = (x + 39)$ MHz.

Table 3. Truth table of output signals for determining reception range of TV tuner.

channel number	CATV	outputs			
		VHF A	VHF B	UHF	GAP
00, 01; 13 to 20;	0	1	0	0	1
70 to 76	1	1	0	0	1
02 to 04	0	1	0	0	0
	1	1	0	0	0
05 to 12	0	0	1	0	0
	1	0	1	0	0
21 to 69	0	0	0	1	0
	1	0	0	1	0
77 to 80	0	1	0	0	1
	1	1	0	0	0
81 to 99	0	0	1	0	1
	1	0	1	0	0

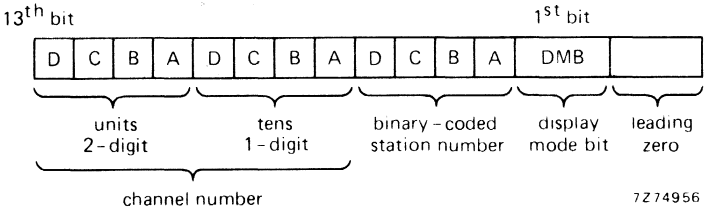


Fig. 4 D-BUS instruction format.

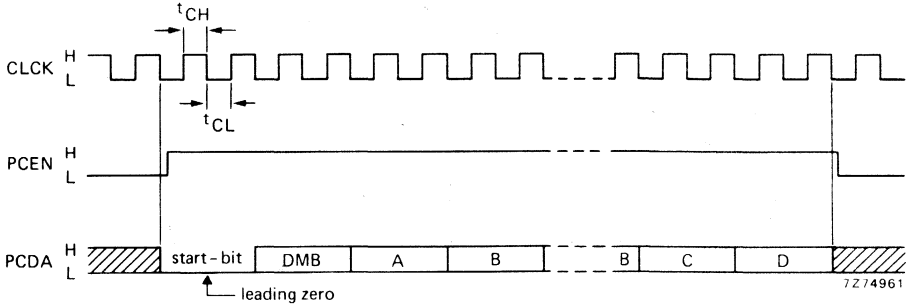


Fig. 5 Timing diagram for channel and station number information on D-BUS.

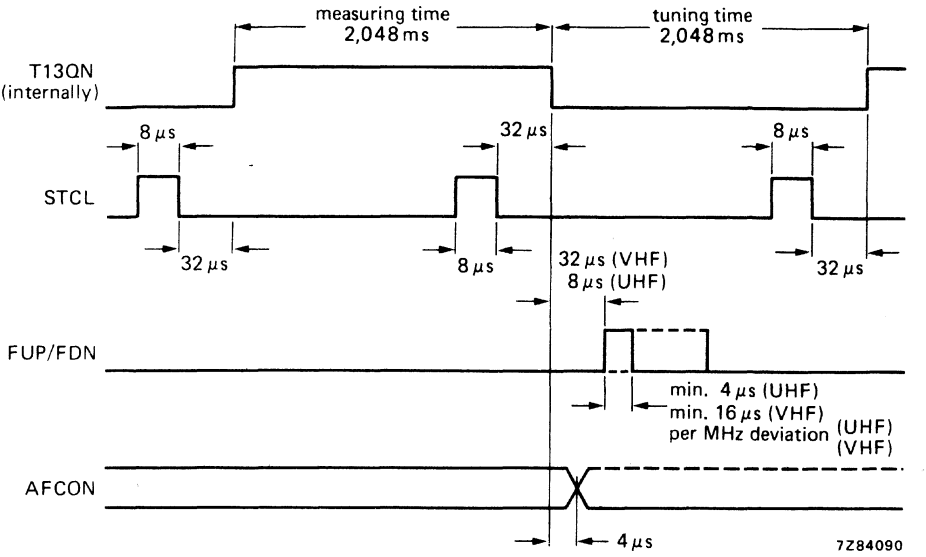
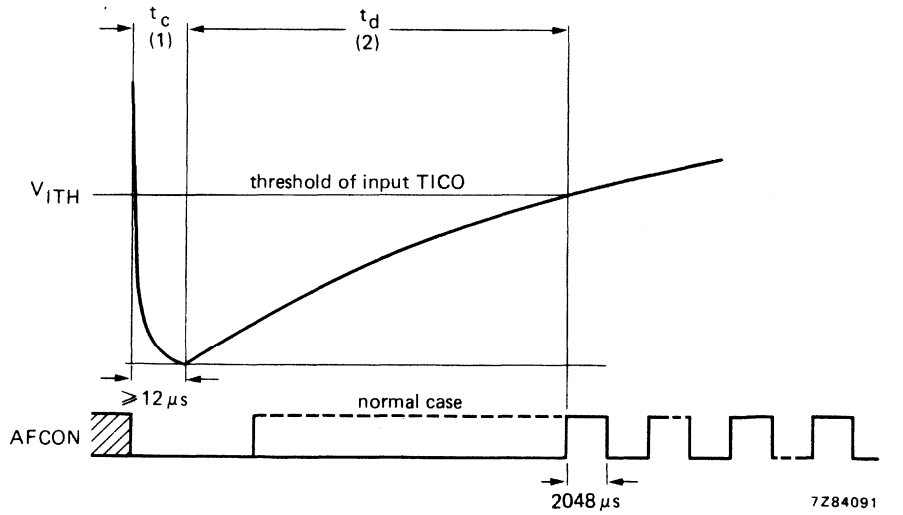


Fig. 6 Timing diagram for signals STCL, FUP, FDN and AFCON.



(1) Minimum time for charging the external capacitor (C).
(2) Delay time for AFCON is HIGH.
Fig. 7 Charging time and delay time waveforms for terminal TICO.
See also Fig. 12.

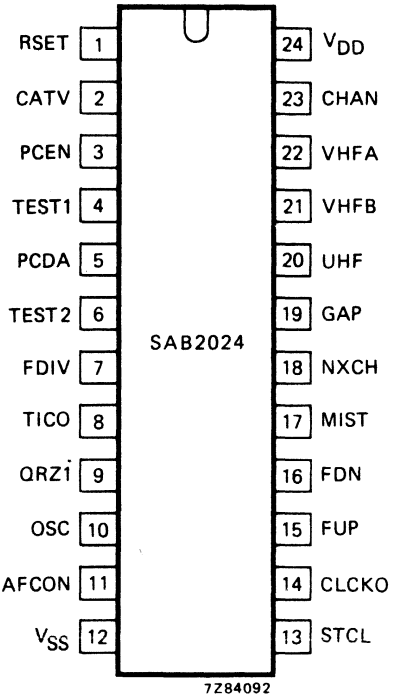


Fig. 8 Pinning diagram.

PINNING

24	V_{DD}	positive supply
12	V_{SS}	negative supply (0 V)

Inputs

1	RSET	reset signal; a HIGH at the input causes zero setting of the whole circuit
2	CATV	enable signal for cable TV channels (see Table 3)
3	PCEN	D-BUS data enable signal
5	PCDA	D-BUS data input
7	FDIV	input for the devided TV tuner oscillator frequency
9	QRZ1	quartz crystal input
17	MIST	control signal for micro-step tuning; ranges 1 to 6
4, 6	TEST1, TEST2	connect to V_{SS}

Input/output

8	TICO	interrupts tuning process; releases control signal (from SAB2015) for micro-step tuning

Outputs

10	OSC	quartz crystal output
11	AFCON	automatic frequency signal; HIGH = AFC on
13	STCL	search tuning clock; repetition rate 2,048 ms
14	CLCKO	system clock; 62,5 kHz
15	FUP	tuning voltage control output for tuner oscillator frequency up
16	FDN	tuning voltage control output for tuner oscillator frequency down
18	NXCH	control signal for channel step during search tuning
19	GAP	identifying signal for unallocated channel numbers during channel search tuning (GAP = HIGH; channel number to be bypassed)
20	UHF	band switch output for UHF band IV/V
21	VHFB	band switch output for VHF band III
22	VHFA	band switch output for VHF band I
23	CHAN	HIGH state indicates channel function: e.g. channel search tuning

RATINGS (V_{SS} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 11	V
Input voltage range	V_I	−0,3 to V_{DD}	V
Input current	$\pm I_I$	max. 10	mA
Output current; all outputs except TICO	$\pm I_O$	max. 10	mA
Output current; TICO	$+I_O$	max. 35	mA
	$-I_O$	max. 10	mA
Power dissipation per output; except TICO	P_O	max. 50	mW
Power dissipation output TICO	P_O	max. 200	mW
Total power dissipation per package	P_{tot}	max. 300	mW
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

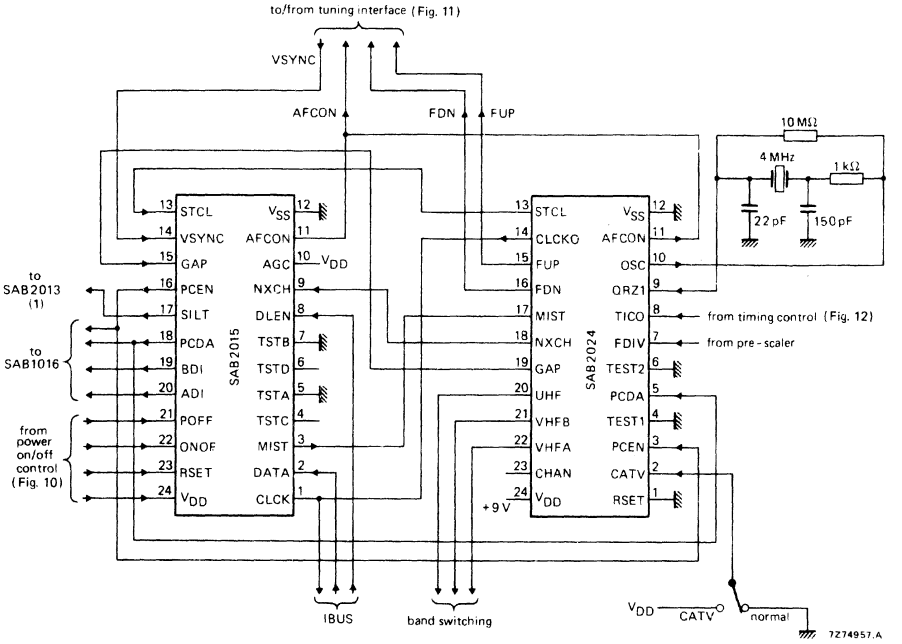
CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	8	9	10	V	
Quiescent current per package	10	I_{DD}	–	–	100	µA	I_O = 0; inputs to V_{DD} or V_{SS}
Input leakage current	10	I_{IR}	–	–	1	µA	T_{amb} = 25 °C; inputs 10 V
		$-I_{IR}$	–	–	1	µA	T_{amb} = 25 °C; inputs V_{SS}
Input voltage LOW	8 to 10	V_{IL}	0	–	$0{,}3V_{DD}$	V	
Input voltage HIGH	8 to 10	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V	
Outputs; except OSZ;CLCKO;TICO							
Output voltage HIGH	8 to 10	V_{OH}	$V_{DD}-1$	–	–	V	$-I_O$ = 0,6 mA
Output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_O = 1,9 mA
Outputs OSZ;CLCKO							
Output voltage HIGH	8 to 10	V_{OH}	$V_{DD}-1$	–	–	V	$-I_O$ = 2,4 mA
Output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_O = 3,8 mA
Output TICO open drain n-channel							
Off-current	10	I_O	–	–	50	µA	V_O = 10 V
Output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_O = 30 mA

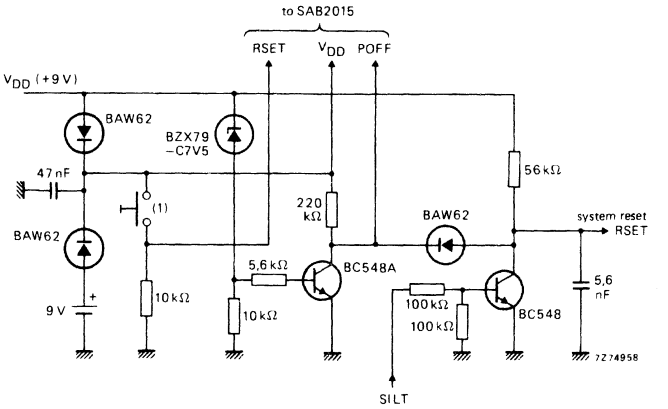
	V_{DD} V	symbol	min.	typ.	max.		conditions
Clock frequency	8 to 10	f_{CLCKO}	–	62,5*	–	kHz	
Input frequency QRZ1; FDIV	8 to 10	f_I	–	–	4,5	MHz	
Duty factor QRZ1; FDIV	8 to 10	δ	0,2	–	0,8		
Input rise/fall time		t_r; t_f	–	–	1	μs	

* Equals $f_{QRZ1}/64$.



(1) Output SILT can be used for muting during channel mode operations and/or dark tuning.

Fig. 9 Interconnection diagram of the SAB2015 and SAB2024 used in a tuner circuit.



(1) Operate button to clear station memory of SAB2015 after battery charge. System reset pulse RSET will remain LOW if tuning operation is in progress.

Fig. 10 Power ON/OFF circuitry; used in combination with Fig. 9.

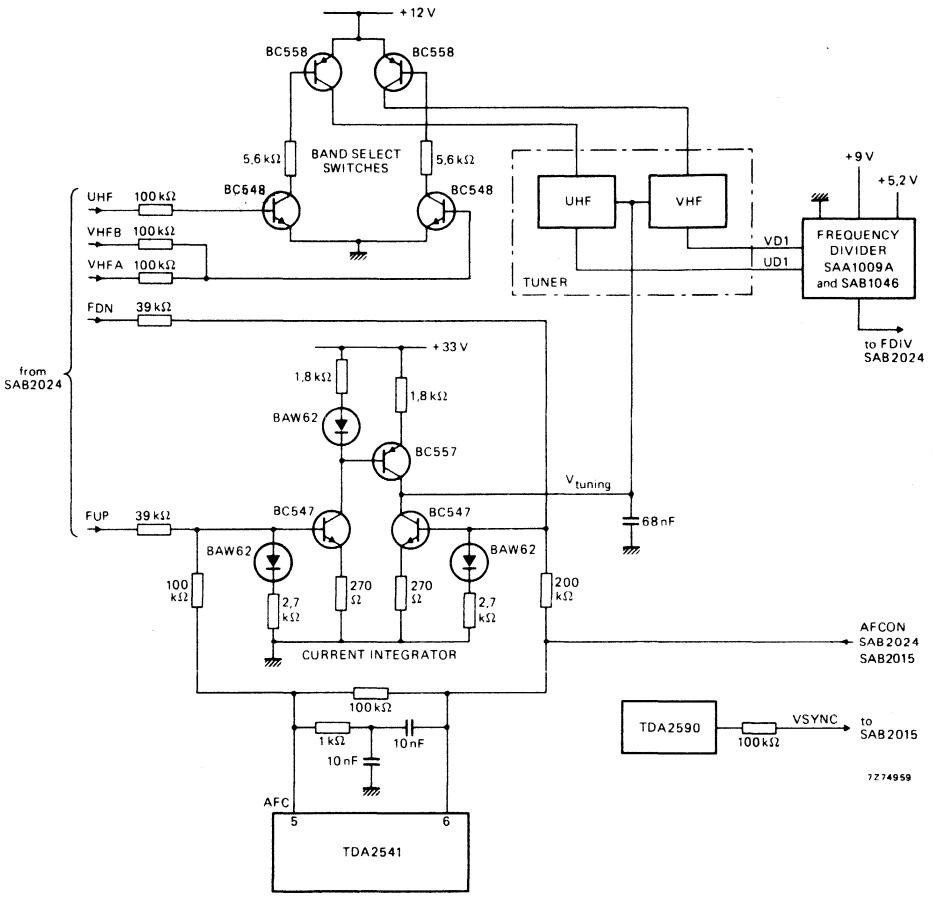
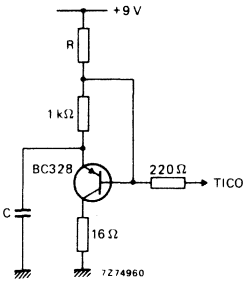


Fig. 11 Tuning interface and band select; used in combination with Fig. 9.



R_{max} = 470 kΩ

C_{max} = 560 nF

$t_{d\,max}$ = 130 ms

$t_{d\,max}$ is the maximum delay which can be obtained under worst-case conditions.

Fig. 12 Tuning constants at input TICO (Fig. 9).

FREQUENCY CONTROL CIRCUIT

for Italian TV channels

The SAB2034 frequency control circuit is identical to the SAB2024 except for the ROM content which is adapted to the Italian channel frequencies.
The proper frequencies for the channels A to L are programmed under the channel numbers 02 to 11 as shown in the ROM content below.

address DICS channel number	video carrier freq. MHz	f_{osc} ROM contents MHz	Italian channel	address DICS channel number	video carrier freq. MHz	f_{osc} ROM contents MHz	Italian channel
00	44,25	83		30	543,25	582	
01	44,25	83		31	551,25	590	
02	53,75	92	A	32	559,25	598	
03	62,25	101	B	33	567,25	606	
04	82,25	121	C	34	575,25	614	
05	175,25	214	D	35	583,25	622	
06	183,75	222	E	36	591,25	630	
07	192,25	231	F	37	599,25	638	
08	201,25	240	G	38	607,25	646	
09	210,25	249	H	39	615,25	654	
10	217,25	256	L	40	623,25	662	
11	224,25	263	E12	41	631,25	670	
12	44,25	83		42	639,25	678	
13	44,25	83		43	647,25	686	
14	44,25	83		44	655,25	694	
15	44,25	83		45	663,25	702	
16	44,25	83		46	671,25	710	
17	44,25	83		47	679,25	718	
18	44,25	83		48	687,25	726	
19	44,25	83		49	695,25	734	
20	44,25	83		50	703,25	742	
21	471,25	510		51	711,25	750	
22	479,25	518		52	719,25	758	
23	487,25	526		53	727,25	766	
24	495,25	534		54	735,25	774	
25	503,25	542		55	743,25	782	
26	511,25	550		56	751,25	790	
27	519,25	558		57	759,25	798	
28	527,25	566		58	767,25	806	
29	535,25	574		59	775,25	814	

N.B. Table continued on next page.

Table continued

address DICS channel number	video carrier freq. MHz	f_{osc} ROM contents MHz	Italian channel	address DICS channel number	video carrier freq. MHz	f_{osc} ROM contents MHz	Italian channel
60	783,25	822		80	44,25	83	
61	791,25	830		81	44,25	83	
62	799,25	838		82	44,25	83	
63	807,25	846		83	44,25	83	
64	815,25	854		84,	44,25	83	
65	823,25	862		85	44,25	83	
66	831,25	870		86	44,25	83	
67	839,25	878		87	44,25	83	
68	847,25	886		88	44,25	83	
69	855,25	894		89	44,25	83	
70	44,25	83		90	44,25	83	
71	44,25	83		91	44,25	83	
72	44,25	83		92	44,25	83	
73	44,25	83		93	44,25	83	
74	44,25	83		94	44,25	83	
75	44,25	83		95	44,25	83	
76	44,25	83		96	44,25	83	
77	44,25	83		97	44,25	83	
78	44,25	83		98	44,25	83	
79	44,25	83		99	44,25	83	

Note: ROM content is $f_{osc} = f_{carrier} + i.f. = x,25 + 38,9 = (x + 39)$ MHz.

REMOTE TRANSMITTER

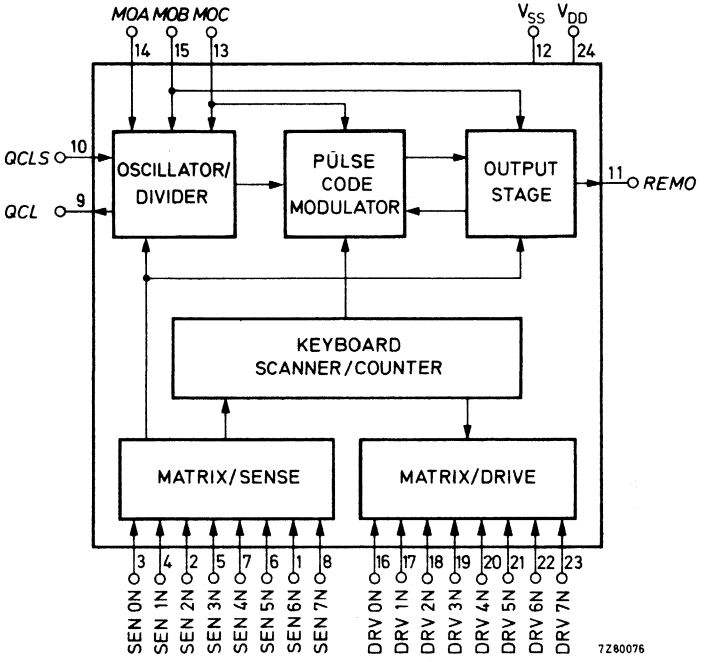


Fig. 1 Block diagram.

Features

- Transmitter for 2 x 64 commands.
- One transmitter for two types of equipment, e.g. radio and television.
- Very low current consumption.
- Particularly suitable for infrared or ultrasonic transmission modes.
- Transmission by means of a pulse code modulation.
- Short interval between operation and re-operation of the same key, due to automatic double word spacing.

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	7 to	10 V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Minimum oscillator input frequency	f_{QCLS}		4 MHz
Quiescent current V_{DD} = 10 V; I_Q = 0; T_{amb} = 25 °C	I_{DD}	typ.	1 μA

PACKAGE OUTLINE

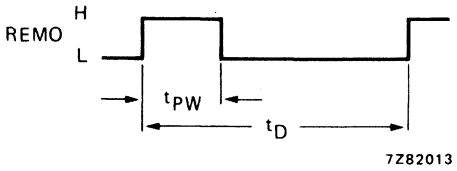
24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

When a key is depressed the oscillator starts running and the keyboard is scanned. The drivers are activated one at a time and during each driver-on period, the sense lines are sequentially scanned. This operation is controlled by the scanning counter such that the value in the counter represents the code of the key being scanned. The counter is stopped when the activated key is located. This mode of operation is particularly free from interference, so the SAB3011 can also be used for AM/FM radio receivers. A serial pulse train is now produced at the signal output (REMO), and is suitable for infrared or ultrasonic transmission. Each operation of a key produces transmission of a double 7-bit data word, in which the binary code elements are represented by different periods between the pulses.
The data word is repeated continually for as long as the key is depressed, at least one repetition. After release of the key, or after the first repetition, the circuit automatically returns to the standby state.

The SAB3011 is specifically designed for battery powered operation. It is fabricated using LOCMOS techniques to provide a circuit that consumes very little power. At standby, with no key operated, the oscillator is switched off, so only leakage currents determine the current consumption; minimum battery load.

The serial pulse code-train used is specially developed for infrared or ultrasonic transmission. Due to the particular requirements of both media on the one hand, and the transmitter elements on the other, there are different pulse formats for the two modes of operation. Application in the local mode differs only very slightly from the infrared operation mode. The principle is the same for all modes of operation. The binary code elements are represented by pulse separations t_D, which follow one another as a series in time. As well as the two pulse separations t_{D0} and t_{D1} used to represent '0' and '1', there are also two further time separations t_{DW} and t_{DS} involved (see Figures 2 and 3). t_{DW} serves to separate words transmitted directly after each other, whilst t_{DS} separates double words when the same key-command is given. The four time separations t_{D0}, t_{D1}, t_{DW} and t_{DS} are in the ratio 9: 11: 14: 19 for ultrasonic mode, and 5: 7: 14: 19 for infrared and local mode.

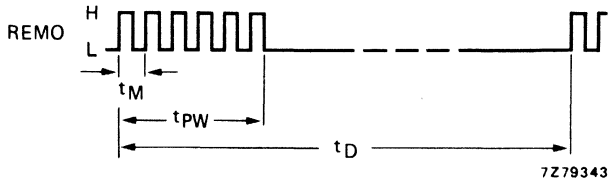


pulse width: $t_{PW} = 3t_{UD}$

unit delay: $t_{UD} = 1{,}024$ ms at $f_Q = 4$ MHz

$t_D = t_{D0} \approx 9t_{UD}$ represents logical '0'
$t_D = t_{D1} \approx 11t_{UD}$ represents logical '1'
$t_D = t_{DW} \approx 14t_{UD}$ word separation
$t_D = t_{DS} \approx 19t_{UD}$ double word separation

Fig. 2 Output signals of the SAB3011 for ultrasonic transmission.



$f_Q = 4$ MHz

$t_Q = \frac{1}{f_Q} = 250$ ns

$t_M = 112t_Q = 28\ \mu s$

$f_M = \frac{1}{t_M} = 35{,}7$ kHz

$t_{PW} = 5{,}5t_M = 154\ \mu s$

$f_{PW} = 6{,}5$ kHz

$t_D = t_{D0} = 5t_{UD}$ represents logical '0'
$t_D = t_{D1} = 7t_{UD}$ represents logical '1'
$t_D = t_{DW} = 14t_{UD}$ word separation
$t_D = t_{DS} = 19t_{UD}$ double word separation

unit delay: $t_{UD} = 4096t_Q = 1{,}024$ ms at $f_Q = 4$ MHz.

Fig. 3 Output signals of the SAB3011 for infrared transmission.

OPERATION DESCRIPTION

Mode programming inputs (MOA, MOB, MOC)

The SAB3011 has several modes of operation like a reset, ultrasonic, infrared, local, test. The operation mode is determined by the inputs MOA, MOB and MOC as shown in Table 1. Input MOC also determines the polarity of the start bits of each command word.

Table 1. Mode programming.

mode inputs MOA	MOB	MOC	mode	start bit S (= MOC)
0	0	0	reset	0
1	0	0	ultrasonic	0
0	1	0	infrared	0
1	1	0	local	0
0	0	1	test	1
1	0	1	ultrasonic	1
0	1	1	infrared	1
1	1	1	local	1

Sense inputs (SEN0N to SEN7N)

These terminals are the sense inputs of the 8 x 8 key-matrix. If no key is operated, all sense inputs are HIGH due to internal pull-up elements.

Driver outputs (DRV0N to DRV7N)

These outputs are drivers for the 8 x 8 key-matrix, and are open-drain n-channel transistors. At standby, all drivers are active; i.e. conductive to V_{SS}. During scanning only one driver at a time is conductive to V_{SS} (low-ohmic), while all the other drivers are high-ohmic. During the output process, a driver remains conductive, if its line locates an operated key.
The arrangement of the IBUS code number for the keyboard is shown in Table 2.

Output (REMO)

The signal output REMO is LOW during standby. During signal transmission, 7 bits are transmitted in the sequence: S, A, B, C, D, E, F. Bit 'S' is a start bit, and is determined by the logic level at MOC (see Table 1). The code of the bits A to F is defined by the 64 key-matrix positions, which are obtained from the crossing-over of the 8 sense inputs and the 8 drive outputs (see Table 2 and Fig. 6).
External circuitry and examples of circuits for infrared and ultrasonic transmission are shown in the section APPLICATION INFORMATION.

Table 2. Arrangement of IBUS code for the keyboard.

SAB3011 inputs		IBUS	SAB3012 IBUS code					
SEN . N	DRV . N	code no.	F	E	D	C	B	A
0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	1
2	0	2	0	0	0	0	1	0
3	0	3	0	0	0	0	1	1
4	0	4	0	0	0	1	0	0
5	0	5	0	0	0	1	0	1
6	0	6	0	0	0	1	1	0
7	0	7	0	0	0	1	1	1
0 to 7	1	8 to 15	0	0	1	000	to	111
0 to 7	2	16 to 23	0	1	0	000	to	111
0 to 7	3	24 to 31	0	1	1	000	to	111
0 to 7	4	32 to 39	1	0	0	000	to	111
0 to 7	5	40 to 47	1	0	1	000	to	111
0 to 7	6	48 to 55	1	1	0	000	to	111
0 to 7	7	56 to 63	1	1	1	000	to	111

Oscillator input (QCLS)/output (QCL)

Input QCLS is the system clock input for local operation. Ouput QCL serves as driver for the oscillator external circuitry (see Fig. 4).

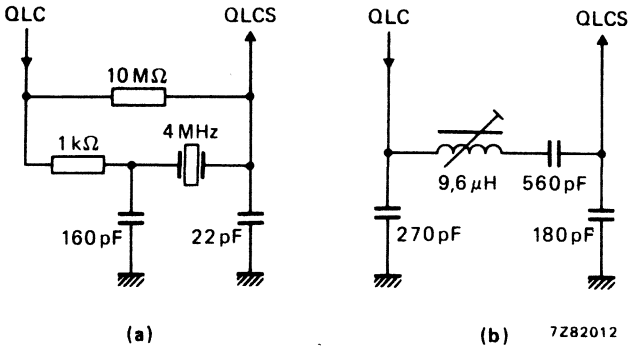


Fig. 4 Typical external oscillator circuitry: (a) crystal oscillator; (b) LC oscillator.

Data for coil in Fig. 4(b):

Frame core: FXC grade 4D1; catalogue no. 3122 104 91480
Screw core: FXC grade 4D1; catalogue no. 3122 104 90590
Coil former: catalogue no. 4312 021 29670
Number of turns: 25 turns enamelled Cu wire (0,08 mm)

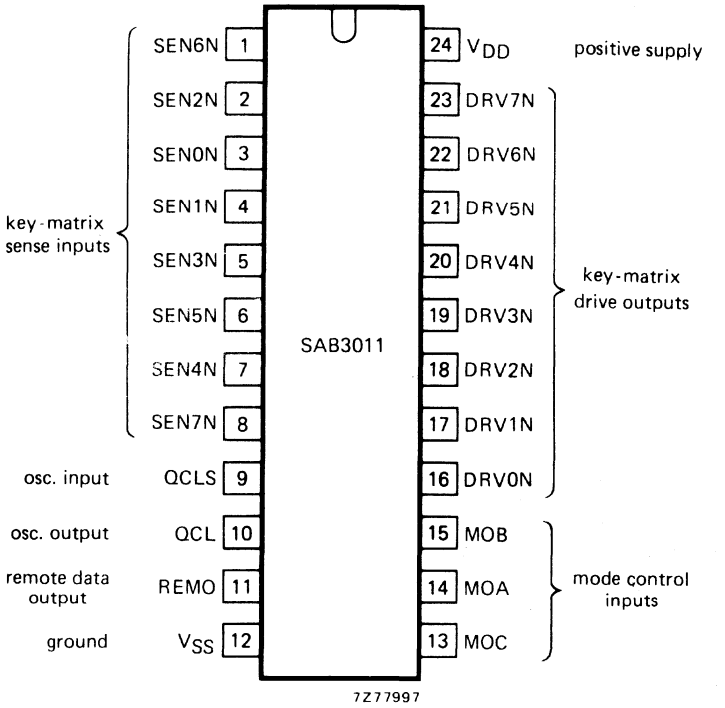


Fig. 5 Pinning diagram.

RATINGS (V_{SS} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 11	V
Input voltage range	V_I	−0,3 to + V_{DD}	V
Input current	I_I	max. 10	mA
Negative input current	$-I_I$	max. 10	mA
Output current	I_O	max. 10	mA
Negative output current	$-I_O$	max. 10	mA
Power dissipation per output	P_O	max. 50	mW
Total power dissipation per package	P_{tot}	max. 300	mW
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	7	–	10	V	
Supply current	10	I_{DD}	–	–	10	µA	I_Q = 0 ** ; $V_{SEN.N} = V_{DD}$
Inputs MOA; MOB; MOC; QCLS							
Input current	10	I_I	–	–	1	µA	V_I = 10 V **
	10	$-I_I$	–	–	1	µA	V_I = 0 V **
Input voltage LOW	7 to 10	V_{IL}	0	–	$0{,}3V_{DD}$	V	
Input voltage HIGH	7 to 10	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V	
Inputs SEN0N to SEN7N *							
Input current	7 to 10	$-I_I$	20	–	250	µA	V_I = 0 V
Input voltage HIGH	7	V_{IH}	$0{,}7V_{DD}$	–	–	V	$-I_I$ = 1 µA **
Output REMO							
Output voltage LOW	7 to 10	V_{QL}	–	–	1	V	I_Q = 1,5 mA
Output voltage HIGH	7 to 10	V_{QH}	$V_{DD}-1$	–	–	V	$-I_Q$ = 2,7 mA
Output QCL							
Output voltage LOW	7 to 10	V_{QL}	–	–	1	V	I_Q = 1,5 mA
Output voltage HIGH	7 to 10	V_{QH}	$V_{DD}-1$	–	–	V	$-I_Q$ = 0,6 mA
Outputs DRV0N to DRV7N open drain n-channel							
Output voltage LOW	7 to 10	V_{QL}	–	–	1	V	I_Q = 1,5 mA
Output leakage current	10	I_Q	–	–	5	µA	V_Q = 10 V
	10	I_Q	–	–	1	µA	V_Q = 10 V **
Input QCLS							
Minimum input frequency	7 to 10	f_{QCLS}	–	–	4	MHz	
Duty factor	7 to 10	δ	0,45	0,5	0,55		f = 4 MHz
Input rise/fall time	7 to 10	t_r; t_f	–	–	50	ns	

* Sense inputs with p-channel pull-up transistor.

** At T_{amb} = 25 °C.

APPLICATION INFORMATION

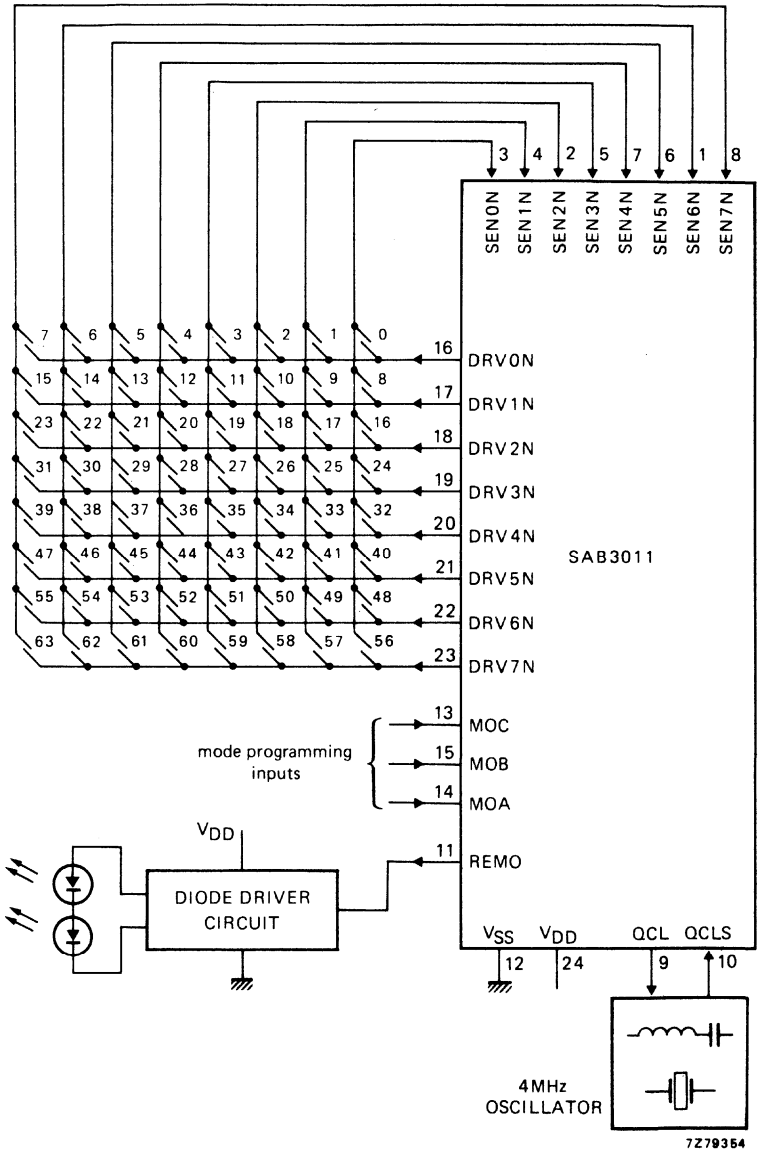


Fig. 6 Typical remote transmitter circuit using SAB3011.

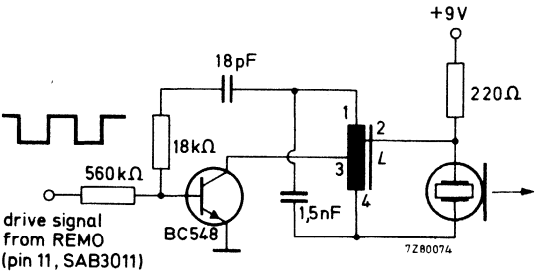


Fig. 7 Ultrasonic transmitter circuit.

Characteristics

f = 40,5 kHz
L_{34} = 10,4 mH
Q = 65
transmission distance: 11 to 14 m

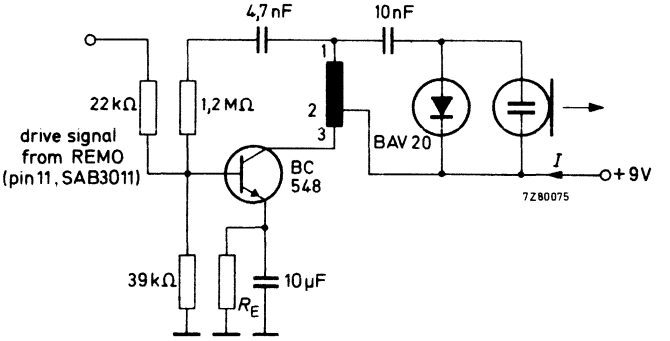


Fig. 8 Ultrasonic transmitter circuit.

Characteristics

f = 40 kHz
L_{13} = 60 mH
Q = 65

R_E Ω	I mA	p (1 m) Pa	transmission distance (m)
1000	5	0,85	10
330	12	1,3	15

APPLICATION INFORMATION (continued)

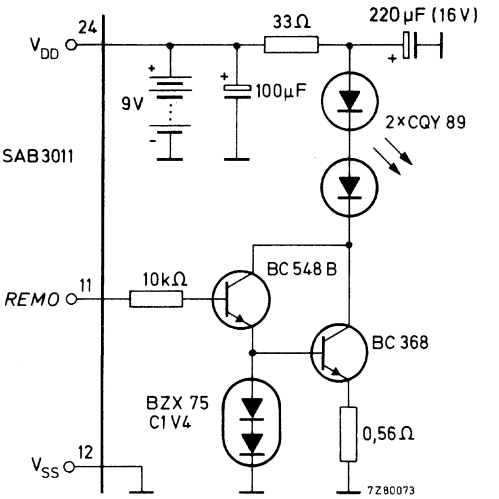


Fig. 9 Infrared transmitter circuit.

RECEIVER AND ANALOGUE MEMORY

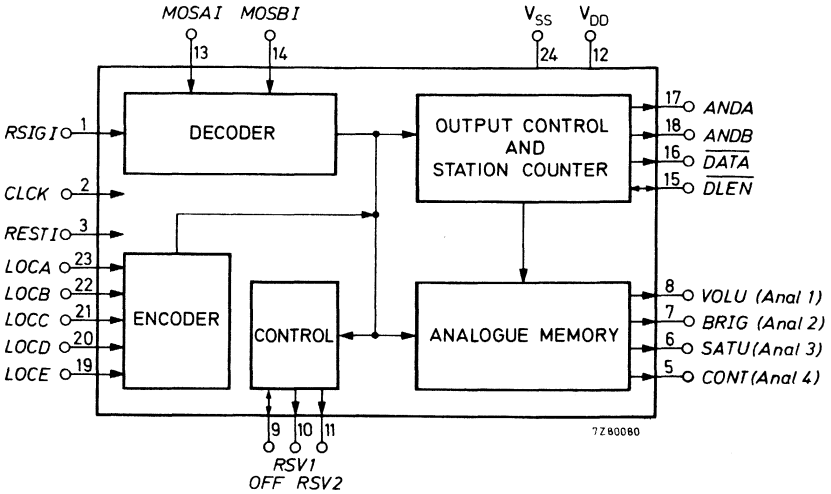


Fig. 1 Block diagram.

Features

- Receiver for 2 x 64 commands in two versions: SAB3012 for TV, SAB3012A for radio.
- 6 + 1 bit code word and the command group (1 bit) are mask programmed.
- Infrared operation: LC or crystal oscillator at the transmitter.
- Ultrasonic operation: crystal oscillator at the transmitter.
- Four 63-step analogue memories with D/A converter; basic setting 28/63.
- Short response time (speed for altering the analogue memories):
  infrared: 115 ms/step; 7,2 s/63 steps.
  ultrasonic: 85 ms/step; 5,4 s/63 steps.
- ON/OFF (standby) output.
- Serial instruction output (IBUS).
- High security against interferences.
- Fast operation, even with the same key, due to double word separation test.
- Inputs for local operation via encoded keys; up to 31 commands.
- Coded outputs for display of analogue signals.
- Supply voltage: 5 V.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Clock frequency	f_{CLCK}	typ.	62,5 kHz
Supply current at V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	typ.	20 mA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The circuit is implemented in N-channel MOS technology. Serial data is derived from the transmitter SAB3011 in remote or extended local operation mode. This data is applied to the RSIGI input, where it is checked and decoded and serially applied as commands to the IBUS. Some commands are also used internally for control of 4 analogue functions and the station memory. Moreover, the circuit has available an input/output for the ON/OFF function, two auxiliary outputs for reserve commands, and the choice of two outputs for control of the on-screen display of the analogue values, or for numeral display control.

For normal local operation, five inputs are available, via which 31 different commands are parallel addressable.

Special features:

- Serial interface for 64 commands.
- Universal control functions for sub-systems: e.g. tuning systems, Teletext, Viewdata, video games, clock with addressable memory etc.
- After operation of a sub-system, the analogue functions and the ON/OFF function remain under direct control.
- Capability for use in an operation mode with parallel station outputs.

OPERATION DESCRIPTION

Remote control data input (RSIGI)

Serial data is derived from the transmitter in remote or local operation mode. This data is applied to the RSIGI input (see Fig. 2), where it is checked and decoded. The instruction bus (IBUS) is then enabled and an output operation takes place.

Response times:
infrared: ≈ 110 ms.
ultrasonic: ≈ 170 ms.

The following tests are carried out for each signal or signal group:

- Dead-time, time between two pulses.
- Word separation.
- Double word separation.

Signals which do not come within the zero or one 'window', restart the input detection procedure. The commands are transmitted as 7-bit words (1 start bit, 6 data bits). The receiver circuit SAB3012 is mask-programmed for start bit S = 0; but a version is also available for radio use, the SAB3012A for S = 1.

Table 1 shows the IBUS-codes.

zero time (t_D)	one time (t_D)	infrared operation mode
5,1 ms ± 1 ms	7,2 ms ± 1 ms	IRA (wide window)
5,1 ms ± 0,13 ms	7,2 ms ± 0,13 ms	IRB (narrow window)

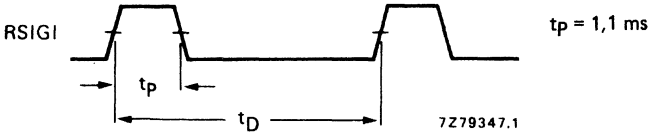
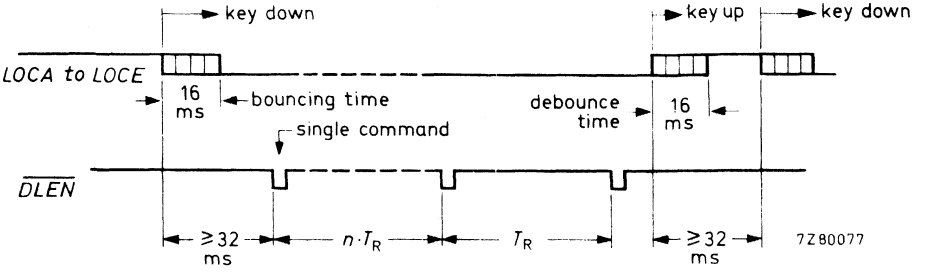


Fig. 2 Specification of the timing of the input signal.

Local keyboard inputs (LOCA, LOCB, LOCC, LOCD and LOCE)

Up to 31 commands (see Table 1) for local control are possible by addressing these 5 inputs from a binary encoded keyboard. A keyboard input (local control) overrides the remote control commands at input RSIGI (from SAB3011). Current IBUS output data is completely isolated.



Repetition rate: 2/second x T_R = 510 ms
8/second x T_R = 129 ms

Fig. 3 Relationship between key operation and command output.

Mode control inputs (MOSAI, MOSBI)

The SAB3012 can decode either infrared or ultrasonic transmission. Pulse code modulation, as used in the SAB3011, offers good performance for a wide range of applications. In view of optimum performance, particularly in respect to the power requirements of the transmitter, pulse widths are matched to the transmission path. This requires a matching of the time window at the receiver in order to achieve the greatest possible freedom from interference.

mode	inputs MOSAI	inputs MOSBI	operation	output	oscillator freq. transmitter	
1	0	0	infrared	IBUS	4 MHz ± 14%	wide window
2	0	1	infrared	IBUS	4 MHz ± 0,8%	small window
3	1	0	ultrasonic	IBUS	4 MHz ± 9%	
4	1	1	infrared	parallel	4 MHz ± 14%	station number register available

Test input (TEST)

Normally grounded.

Table 1. Specifications of the IBUS-code

RSIGI/ IBUS code no.	inputs					instruction code							outputs											
	LOCE	LOCD	LOCC	LOCB	LOCA	F	E	D	C	B	A	CL.*	OFF	RSV1	RSV2	VOLU	ANAL2	ANAL3	ANAL4	ANDA	ANDB	PRCD	PRCC	PRCB	PRCA
0						0	0	0	0	0	0	S				29/ 63	29/ 63	29/ 63	29/ 63						
1						0	0	0	0	0	1	S	0			0				0	0				
2						0	0	0	0	1	0	S	1												
3						0	0	0	0	1	1	S		0/1											
4						0	0	0	1	0	0	R8	0												
5	1	1	0	1	0	0	0	0	1	0	1	S	0												
6						0	0	0	1	1	0	S			⎍										
7						0	0	0	1	1	1	S			⎍										
8						0	0	1	0	0	0	R8													
9						0	0	1	0	0	1	R8													
10						0	0	1	0	1	0	R8													
11						0	0	1	0	1	1	R8													
12						0	0	1	1	0	0	R8													
13						0	0	1	1	0	1	R8													
14						0	0	1	1	1	0	R8													
15						0	0	1	1	1	1	R8													
16	0	0	1	0	1	0	1	0	0	0	0	S	0			⎍						1	1	1	1
17	0	0	1	0	0	0	1	0	0	0	1	S	0			⎍						0	0	0	0
18	0	0	1	1	1	0	1	0	0	1	0	S	0			⎍						0	0	0	1
19	0	0	1	1	0	0	1	0	0	1	1	S	0			⎍						0	0	1	0
20	0	0	0	0	1	0	1	0	1	0	0	S	0			⎍						0	0	1	1
21	0	0	0	0	0	0	1	0	1	0	1	S	0			⎍						0	1	0	0
22	0	0	0	1	1	0	1	0	1	1	0	S	0			⎍						0	1	0	1
23	0	0	0	1	0	0	1	0	1	1	1	S	0			⎍						0	1	1	0
24	0	1	1	0	1	0	1	1	0	0	0	S	0			⎍						0	1	1	1
25	0	1	1	0	0	0	1	1	0	0	1	S	0			⎍						1	0	0	0
26	0	1	1	1	1	0	1	1	0	1	0	S	0			⎍						1	0	0	1
27	0	1	1	1	0	0	1	1	0	1	1	S	0			⎍						1	0	1	0
28	0	1	0	0	1	0	1	1	1	0	0	S	0			⎍						1	0	1	1
29	0	1	0	0	0	0	1	1	1	0	1	S	0			⎍						1	1	0	0
30	0	1	0	1	1	0	1	1	1	1	0	S	0			⎍						1	1	0	1
31	0	1	0	1	0	0	1	1	1	1	1	S	0			⎍						1	1	1	0

* Instruction class (CL.): S = single
R8 = repeat ≈ 8/second

⎍ : mute control

IBUS code no.	SAB3012	SAB2013	SAB2015
0	basic set analogue	basic set analogue	–
1	mute/on	mute/on	display of mode (2,5 s)
2	off	off	mode reset
3	reserve A	–	–
4	on	on	display of mode (2,5 s)
5	on	on	search tuning up
6	reserve B	–	–
7	reserve C		
8	–	volume up	–
9	–	volume down	–
10	–	brightness up	–
11	–	brightness down	–
12	–	saturation up	–
13	–	saturation down	–
14	–	contrast up	–
15	–	contrast down	–
16	on	on	station 16/0
17	on	on	1/1
18	on	on	2/2
19	on	on	3/3
20	on	on	4/4
21	on	on	5/5
22	on	on	6/6
23	on	on	7/7
24	on	on	station 8/8
25	on	on	9/9
26	on	on	10/–
27	on	on	11/–
28	on	on	12/–
29	on	on	13/–
30	on	on	14/–
31	on	on	15/–

Table 1. Specification of the IBUS-code (continued)

RSIGI/ IBUS code no.	inputs					instruction code							outputs												
	LOCE	LOCD	LOCC	LOCB	LOCA	F	E	D	C	B	A	CL.*	OFF	RSV1	RSV2	VOLU	ANAL2	ANAL3	ANAL4	ANDA	ANDB	PRCD	PRCC	PRCB	PRCA
32	1	1	1	0	1	1	0	0	0	0	0	S	–												
33	1	1	1	0	0	1	0	0	0	0	1	S													
34	1	1	1	1	0	1	0	0	0	1	0	S	0												
35						1	0	0	0	1	1	S	**0**												
36	1	1	0	0	1	1	0	0	1	0	0	R2	0			⊔						X	X	X	X
37	1	1	0	0	0	1	0	0	1	0	1	R2	0			⊔⊔						X	X	X	X
38	1	1	0	1	1	1	0	0	1	1	0	R2	0			⊔⊔									
39						1	0	0	1	1	1	R2	0			⊔									
40	1	0	1	0	1	1	0	1	0	0	0	R8				→1				0	0				
41	1	0	1	0	0	1	0	1	0	0	1	R8				→0				0	0				
42	1	0	1	1	1	1	0	1	0	1	0	R8					→1			0	1				
43	1	0	1	1	0	1	0	1	0	1	1	R8					→0			0	1				
44	1	0	0	0	1	1	0	1	1	0	0	R8						→1		1	0				
45	1	0	0	0	0	1	0	1	1	0	1	R8						→0		1	0				
46	1	0	0	1	1	1	0	1	1	1	0	R8							→1	1	1				
47	1	0	0	1	0	1	0	1	1	1	1	R8							→0	1	1				
48						1	1	0	0	0	0	S													
49						1	1	0	0	0	1	S													
50						1	1	0	0	1	0	S													
51						1	1	0	0	1	1	S													
52						1	1	0	1	0	0	R8													
53						1	1	0	1	0	1	R8													
54						1	1	0	1	1	0	R8													
55						1	1	0	1	1	1	R8													
56						1	1	1	0	0	0	R8													
57						1	1	1	0	0	1	R8													
58						1	1	1	0	1	0	R8													
59						1	1	1	0	1	1	R8													
60						1	1	1	1	0	0	R8													
61						1	1	1	1	0	1	R8													
62						1	1	1	1	1	0	R8													
63						1	1	1	1	1	1	R8													

* Instruction class (CL.): S = single
R2 = repeat ≈ 2/second
R8 = repeat ≈ 8/second

⊔ : mute control

X : change of station counter

IBUS code no.	SAB3012	SAB2013	SAB2015
32	–		display on/off
33	–		store
34	on	on	channel mode
35	on	on	search tuning down
36	on	on	step station up
37	on	on	step station down
38	on	on	step channel up
39	on	on	step channel down
40	volume up	–	–
41	volume down	–	–
42	brightness up	–	–
43	brightness down	–	–
44	saturation up	–	–
45	saturation down	–	–
46	contrast up	–	–
47	contrast down	–	–
48	–	–	–
49	–	–	–
50	–	–	–
51	–	–	–
52	–	–	–
53	–	–	–
54	–	–	–
55	–	–	–
56	–	–	–
57	–	–	–
58	–	–	–
59	–	–	–
60	–	–	–
61	–	–	–
62	–	–	–
63	–	–	–

IBUS outputs

Outputs $\overline{DATA}$ and $\overline{DLEN}$ are inverted.

Proper commands are available for the duration of a key operation as a single command or repeated commands, in accordance with the sub-system requirements (see Table 1). The following output modes are provided:

- Single command; e.g. digits.
- Repetition rate: 2/second; e.g. step functions.
- Repetition rate: 8/second; e.g. analogue functions.

The IBUS command is available at output $\overline{DATA}$ synchronous with the system clock; the word length is 7 bits, one start bit and 6 data bits.

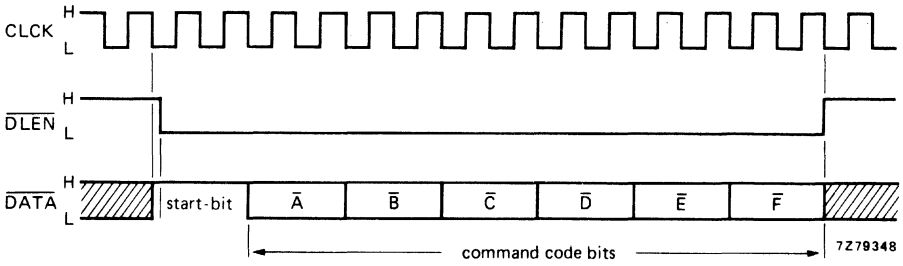


Fig. 4 Output waveforms of a command transmission.

Various word formats can be transmitted between the sub-systems, so it is necessary that each receiver should carry out recognition of a word format. Word formats which do not correspond with the requirements have no effect on the system. It is also necessary that all sub-systems which receive or supply information to the BUS-line should check whether or not the BUS is occupied, if yes, the output is delayed. Output $\overline{DLEN}$ acts as an input for this procedure. The output delay amounts to $7 \times t_{CLK} = 112\ \mu s$.

Analogue memories

The SAB3012 contains four 63-step memories for analogue functions. The speed of stepping depends upon the transmission rate of the remote control; e.g.:

infrared transmission: 115 ms/step.
ultrasonic transmission: 85 ms/step.

Stepping through the full range takes:

infrared transmission: 7,2 seconds.
ultrasonic transmission: 5,4 seconds.

When operating in the local mode, via inputs LOCA to LOCE, the stepping speed is 129 ms/step; 8,1 seconds for the full range.

The analogue values are represented by rectangular pulses of 1 kHz; the duty factor determines the analogue values. The analogue voltage is available at the output of an externally connected low-pass filter.

The command (0) 'basic setting' presets the analogue memory to a mid-position (29/63).

After switching-on the supply, the analogue memories are preset via input RESTI to position 29/63.

The volume control output (VOLU) is set LOW, respectively enabled by the toggle command mute (1). The volume output will be set LOW for a short period T_S (see Fig. 5) by the following commands:

step 16 to 31.
station 1 to 16/0 to 9.
step 36 to 39; station step up/down and channel step up/down.

Muting will be reset by the following commands:

mute command (1).
volume up command (40); the volume output increases starting from LOW.
basic setting command (0).
OFF command (2).

In the standby mode, output OFF = HIGH, the analogue memories cannot be changed.

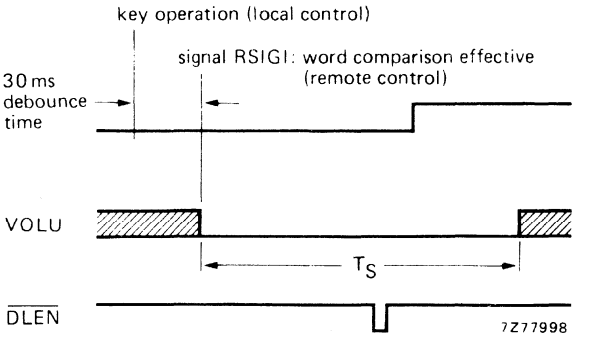


Fig. 5 Timing diagram for muting at station and channel selection.

RSIGI mode (from SAB3011)	T_S
infrared transmission	230 ms
ultrasonic transmission	170 ms
local operation	260 ms

Input/output OFF

OFF is the output of a flip-flop (ON/OFF-flag). If this output is LOW, the system is in the ON-mode; if HIGH, the system is standby (OFF). The system is set to the standby mode by a reset at input RESTI. Terminal OFF operates as an input in standby. Forcing to LOW (set time $\geqslant 32\ \mu s$) makes the chip operational, e.g. switching on via a wiping contact on the mains switch.

Reserve outputs (RSV1 and RSV2)

RSV1 is the output of a flip-flop, which toggles after the proper received command reserve A (3). The output is also set LOW by a reset at the input RESTI.

RSV2 generates a single pulse by the command reserve B (6); duration of the pulse:

RSIGI mode (from SAB3011)	T_{RSV2}
infrared transmission	110 ms
ultrasonic transmission	85 ms

Command reserve C (7) sets RSV2 HIGH with a duration of a key-down operation; error-free reception is assumed.

Display of analogue values outputs (ANDA and ANDB)

Both outputs carry information concerning the changes in an analogue function. This information can be used to control the display of the analogue function.
Some examples of display:

- Bar graphs with changing colour identification.
- Multiple bar graphs.
- Numerical display of the activated analogue function.
- Multiple numerical display of the analogue values.

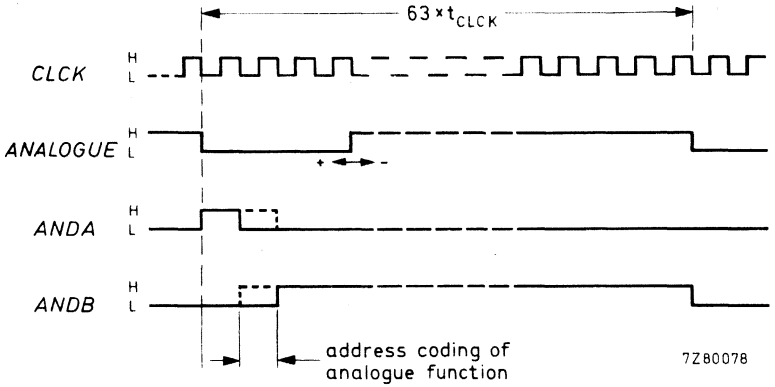


Fig. 6 Output signals for display applications.

Analogue memory states:

analogue function	ANDA	ANDB
VOLUME	0	0
ANAL2	0	1
ANAL3	1	0
ANAL4	1	1

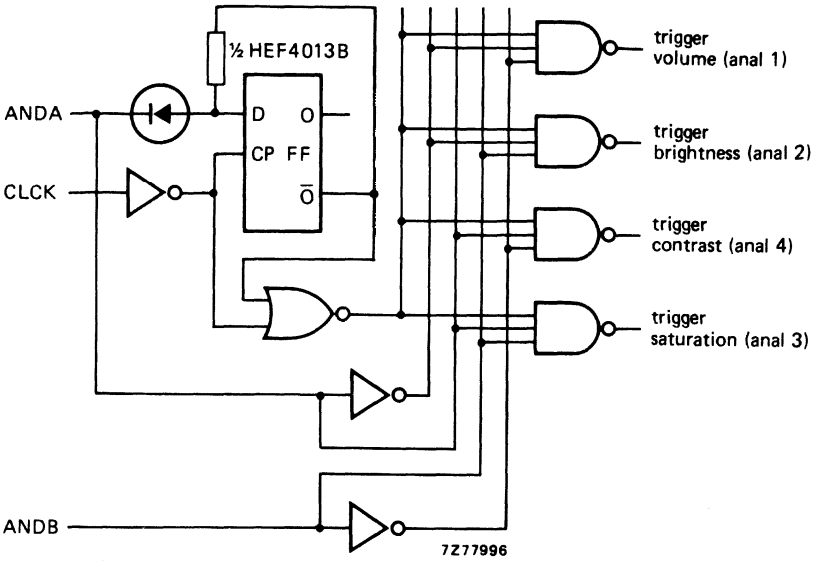


Fig. 7 Example of a circuit showing the generation of the analogue signals.

Internal station counter outputs (PRCA, PRCB, PRCC, PRCD)

By applying a HIGH level to inputs MOSAI and MOSBI, the outputs ANDA, ANDB, $\overline{\text{DATA}}$ and $\overline{\text{DLEN}}$ are switched-over internally to the station counter.
The following arrangement has been made:

terminal	station counter
ANDA	PRCA
ANDB	PRCB
$\overline{\text{DATA}}$	PRCC
$\overline{\text{DLEN}}$	PRCD

The station counter outputs are coded as shown in Table 1.

If the station counter contains a command, the volume output (VOLU) is set LOW for a short period (mute). The change of the station counter is obtained during the mute period (see Fig. 5).

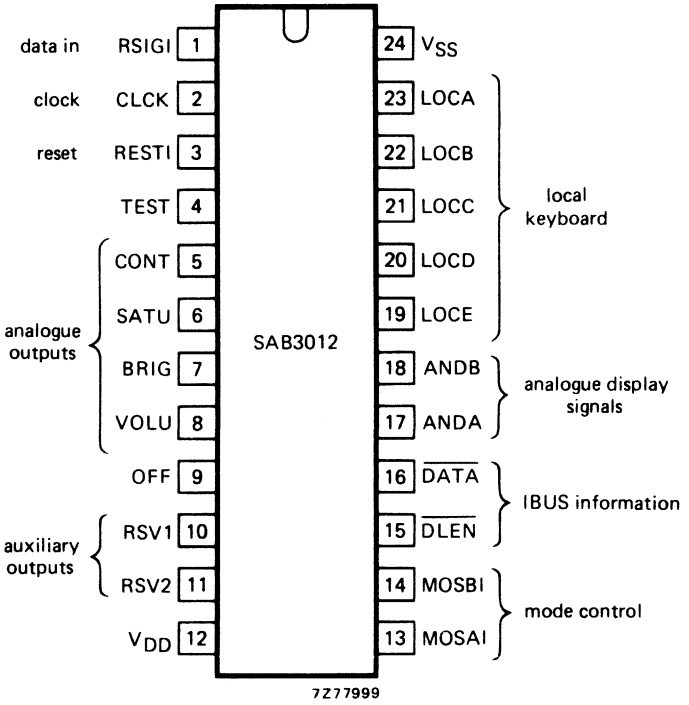


Fig. 8 Pinning diagram.

RATINGS (V_{SS} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	max.	7,5	V
Input voltage	V_I	max.	15	V
Input current	I_I	max.	10	mA
Negative input current	$-I_I$	max.	10	mA
Output current	I_O	max.	10	mA
Negative output current	$-I_O$	max.	10	mA
Power dissipation per output	P_O	max.	50	mW
Total power dissipation per package	P_{tot}	max.	500	mW
Operating ambient temperature range	T_{amb}	−20 to + 70		°C
Storage temperature range	T_{stg}	−55 to + 150		°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	4,5	5,0	5,5	V	
Supply current	5	I_{DD}	–	–	25	mA	
Input leakage current	5	I_{IR}	–	–	1	μA	V_I = –0,3 to + 10 V
Input voltage LOW	5	V_{IL}	–0,3	–	0,8	V	
Input voltage HIGH	5	V_{IH}	3,5	–	10	V	
Outputs $\overline{DATA}$, $\overline{DLEN}$, OFF, RSV1,RSV2,ANDA,ANDB							
Output voltage open drain; LOW	5	V_{QL}	–	–	1	V	I_{QL} = 2,5 mA
Output voltage HIGH	5	V_{QH}	–	–	15	V	I_{QH} = 20 μA
Outputs VOLU, BRIG, CONT, SATU							
Output voltage open drain; LOW	5	V_{QL}	–	–	1	V	I_{QL} = 6 mA
Output voltage HIGH	5	V_{QH}	–	–	15	V	I_{QH} = 20 μA
Input OFF current set to standby mode	5	I_{OFF}	15	–	–	mA	$V_{QL} \rightarrow V_{QH}$
Clock frequency	5	f_{CLCK}	56,25	62,5	68,75	kHz	
Duty factor	5	δ	0,4	0,5	0,6	–	
Input rise/fall time	5	t_r; t_f	–	–	1	μs	

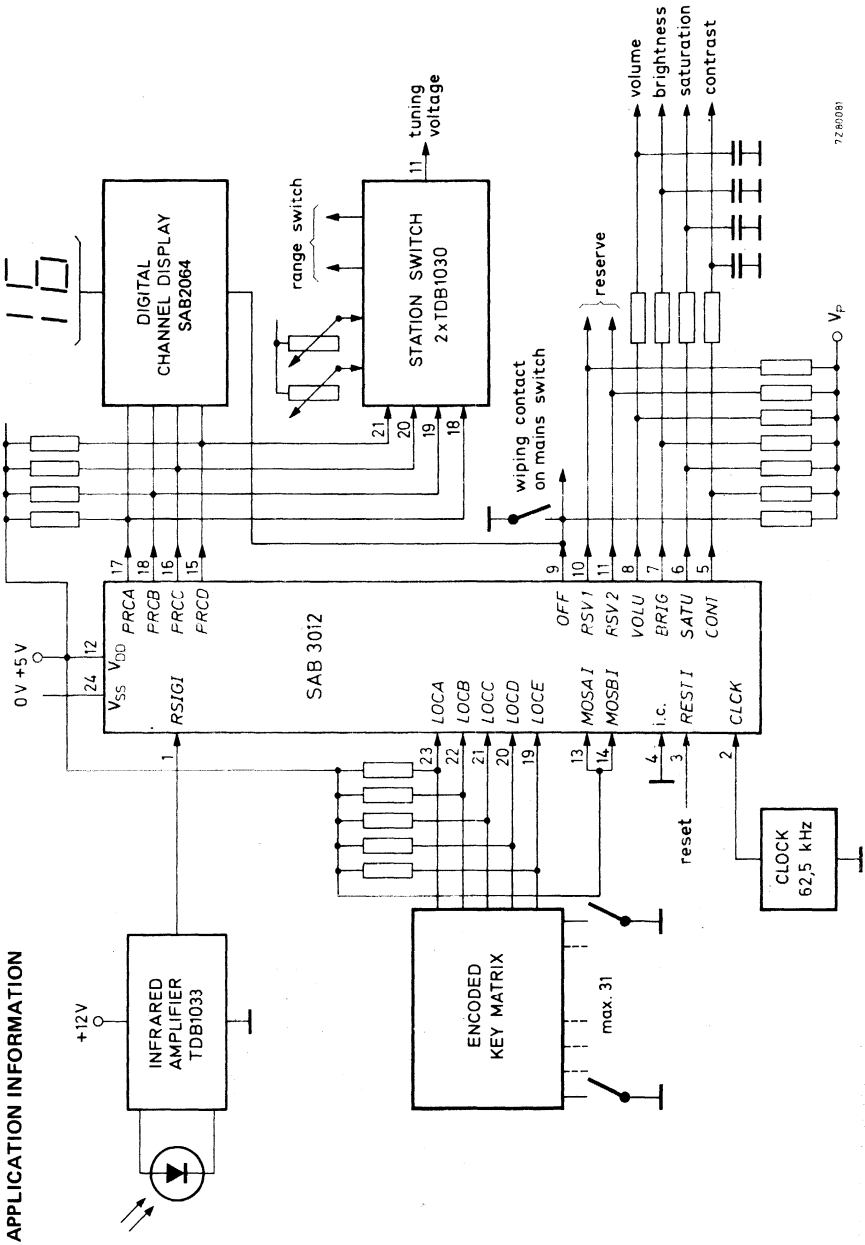


Fig. 9 Typical receiver circuit using the SAB3012 with station output.

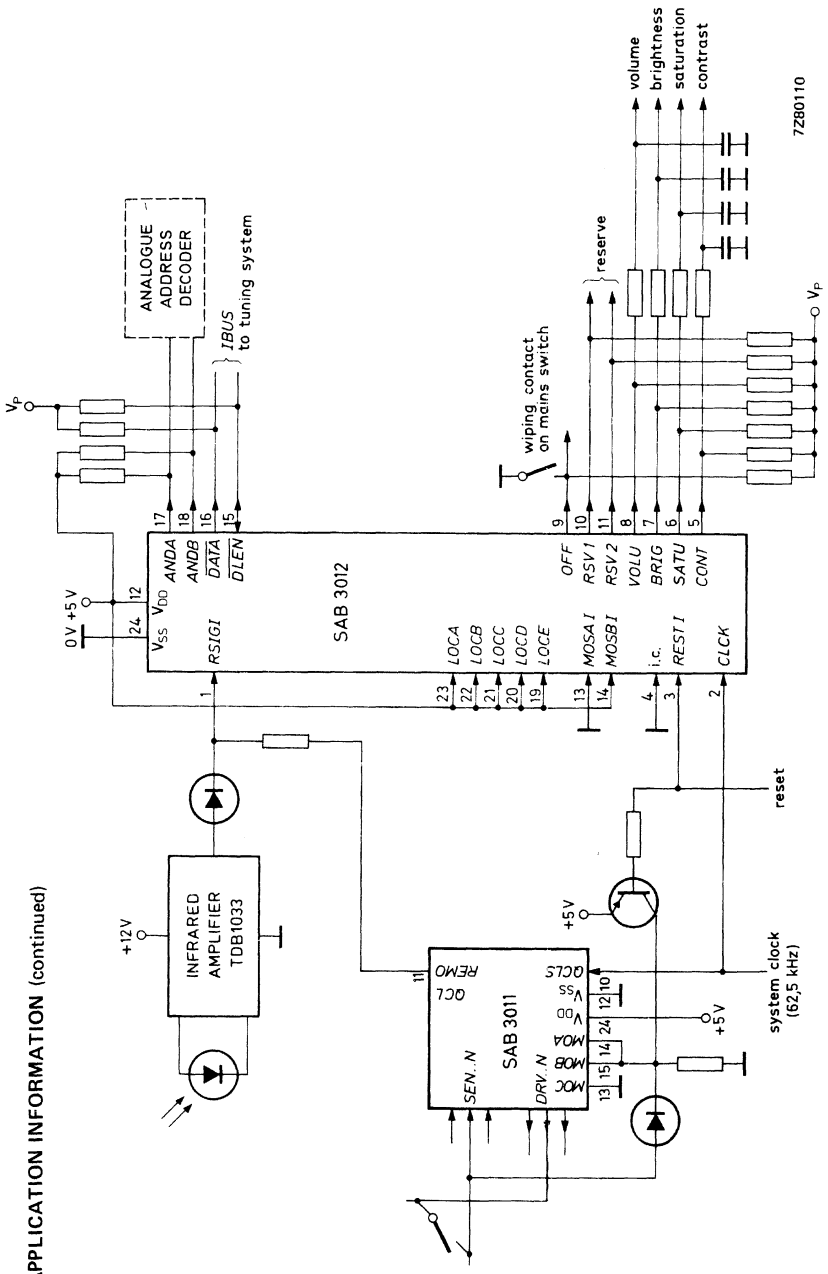
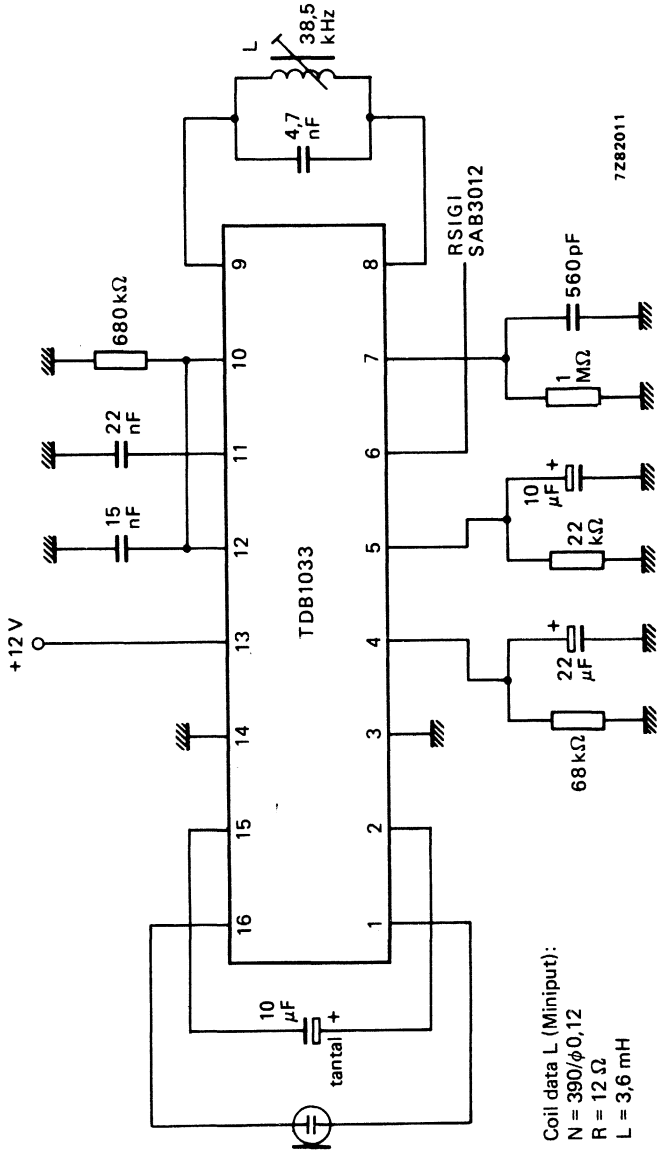


Fig. 10 Typical receiver circuit using the SAB3012 and SAB3011 for local control.

APPLICATION INFORMATION (continued)



Coil data L (Miniput):
N = 390/ϕ0,12
R = 12 Ω
L = 3,6 mH

Fig. 11 Ultrasonic receiver amplifier circuit using TDB1033.

6-FUNCTION ANALOGUE MEMORY; MICROCOMPUTER CONTROLLED

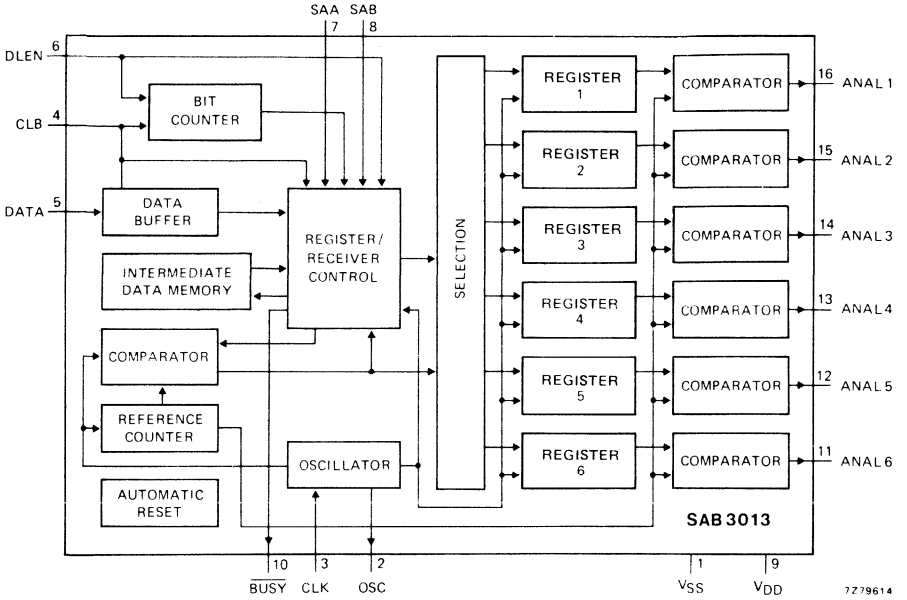


Fig. 1 Block diagram.

Features

- 6-function analogue memory; D/A converter with 6-bit resolution.
- The output of the analogue values is pulse-width modulated with adjustable repetition rate (max. 15 kHz).
- Microcomputer-adapted asynchronous serial interface for data input (CBUS).
- Parallel operation of up to four SAB3013 circuits is possible.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Clock frequency	f_{CLK}	<	1 MHz
Quiescent current; V_{DD} = 5 V; I_Q = 0; T_{amb} = 25 °C	I_{DD}	typ.	35 mA

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

GENERAL DESCRIPTION

The SAB3013 is designed to deliver analogue values in microcomputer-controlled television receivers and radio receivers. The circuit comprises an analogue memory and D/A converter for 6 analogue functions with a 6-bit resolution for each. The information for the analogue memory is transfered by the microcomputer via an asynchronous serial data bus.
The SAB3013 accomplishes a word format recognition, so it is able to operate one common data bus together with circuits having different word formats.
The data word of the microcomputer used for the SAB3013 consists of information for addressing the appropriate SAB3013 circuit (2-bits), for addressing the analogue memories concerned (3-bits) and processing of the wanted analogue value (6-bits). The address of the circuit is externally programmable via two inputs. It is possible to address up to four SAB3013 circuits via one common bus.
The built-in oscillator can be used for a frequency between 30 kHz and 1 MHz. The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ (max. 15,6 kHz at f_{CLK} = 1 MHz), and the analogue values are determined by the ratio of the HIGH-time and the cycle time. A d.c. voltage proportional to the analogue value is obtained by means of an external integration network (low-pass filter).

OPERATION DESCRIPTION

The data input is achieved serially via the inputs DATA, DLEN and CLB. Clock pulses have to be applied at input CLB for data processing at input DATA. Data processing is only possible when DLEN = HIGH. Received data are only accepted by the intermediate data memory, when a transmission is offered, which is required for the SAB3013:

- 12 clock pulses must be received at input CLB (word format control) during transmission (DLEN = HIGH).
- The start-bit must be LOW.
- The system address bits must be A = SAA and B = SAB.

The data word for the SAB3013 consists of the following bits (see Fig. 2):

1 start-bit
2 system address bits (A and B)
3 address bits for selection of the wanted analogue memory
6 data bits for processing the analogue value

The acceptance in the intermediate data memory and processing to the analogue memory are caused by a load pulse at input CLB (DLEN = LOW). Ouput $\overline{BUSY}$ = LOW during the transfer time (t_{BUSY} is max. 64 x t_{CLK}).

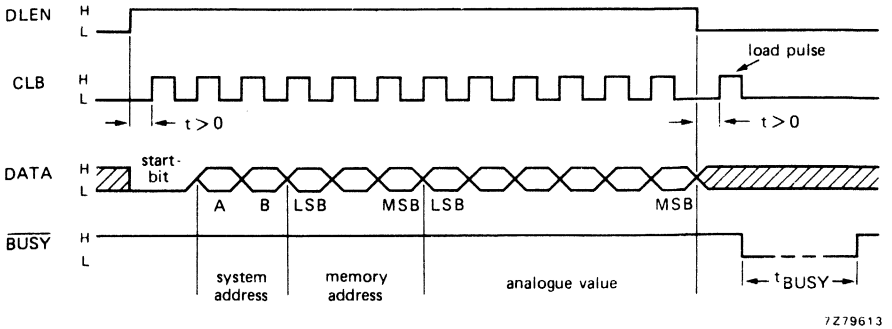


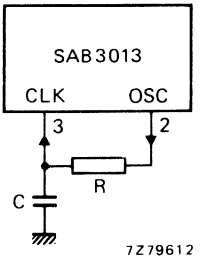
Fig. 2 Waveforms showing a CBUS transmission.

Address inputs (SAA, SAB)

The address of the SAB3013 is programmed at the inputs SAA and SAB. These inputs must be externally wired HIGH or LOW; they may not be left disconnected.

Oscillator inputs (CLK, OSC)

The oscillator frequency is determined by the external circuitry to the terminals CLK and OSC as shown in Fig. 3. Instead of this circuitry an externally generated oscillator signal can be connected to input CLK.



For f_{CLK} = 1 MHz: R = 27 kΩ; C = 27 pF.

Fig. 3 Application advice for the oscillator.

Analogue outputs (ANAL1 to ANAL6)

The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ at the outputs ANAL1 to ANAL6. The analogue value is determined by the ratio of the HIGH-time and the cycle time (values between 1/64 and 64/64 can be obtained).

Reset

The circuit generates internally a reset-cycle with a duration of one clock cycle after switching on the supply, providing that the interruption of the supply was not longer than 25 μs. All analogue memories are set to 50% (analogue value 32/64) after the reset-cycle.

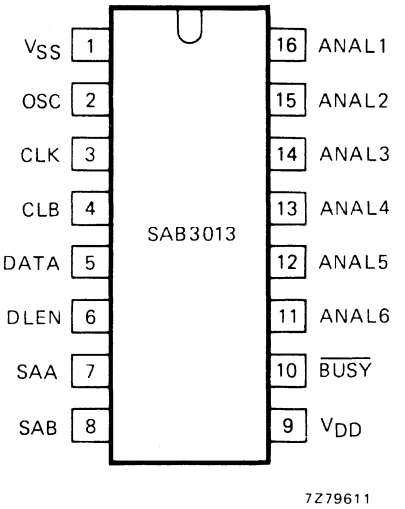


Fig. 4 Pinning diagram.

PINNING

1	V_{SS}	negative supply (0 V)	
9	V_{DD}	positive supply	
4	CLB	asynchronous clock pulse	CBUS
5	DATA	data input	CBUS
6	DLEN	data line enable input	CBUS
7	SAA	address inputs	
8	SAB	address inputs	
2	OSC	oscillator output	
3	CLK	oscillator input (Schmitt-trigger)	
16	ANAL1	analogue outputs	
15	ANAL2	analogue outputs	
14	ANAL3	analogue outputs	
13	ANAL4	analogue outputs	
12	ANAL5	analogue outputs	
11	ANAL6	analogue outputs	
10	$\overline{BUSY}$	output	

RATINGS

Limiting values in accordance to the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 15	V
Input voltage range	V_I	−0,3 to + 15	V
Input current	$\pm I_I$	max. 100	μA
Output current	$\pm I_O$	max. 10	mA
Power dissipation per output	P_O	max.	mW
Total power dissipation per package	P_{tot}	max.	mW
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−10 to + 85	°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.	conditions
Supply voltage		V_{DD}	4,5	5	5,5 V	
Supply current	5	I_{DD}	–	–	35 mA	
Inputs DATA, CLB, DLEN, SAA, SAB						
Input voltage LOW	5	V_{IL}	−0,3	–	0,8 V	
Input voltage HIGH	5	V_{IH}	3,5	–	12 V	
Input leakage current	5	I_{IR}	–	–	1 μA	V_I = −0,3 to + 12 V
Outputs ANAL1 to ANAL6; $\overline{BUSY}$ (open drain)						
Output voltage LOW	5	V_{OL}	–	–	1 V	I_O = 6 mA
Output leakage current	5	I_{OR}	–	–	20 μA	V_{OH} = 15 V
Input CLK						
Input leakage current	5	I_{IR}	–	–	1 μA	V_I = −0,3 to 12 V
Clock frequency	5	f_{CLK}	0,03	–	1 MHz	
Inputs DATA, DLEN, CLB						
Pulse duration HIGH	5	t_{WH}	400	–	– ns	
Pulse duration LOW	5	t_{WL}	400	–	– ns	
Input frequency CLB	5	f_{CLB}	0	–	1 MHz	
Input rise/fall time	5	t_r; t_f	–	–	1 μs	

DEVELOPMENT SAMPLE DATA

IBUS SUB-SYSTEM INTERFACE

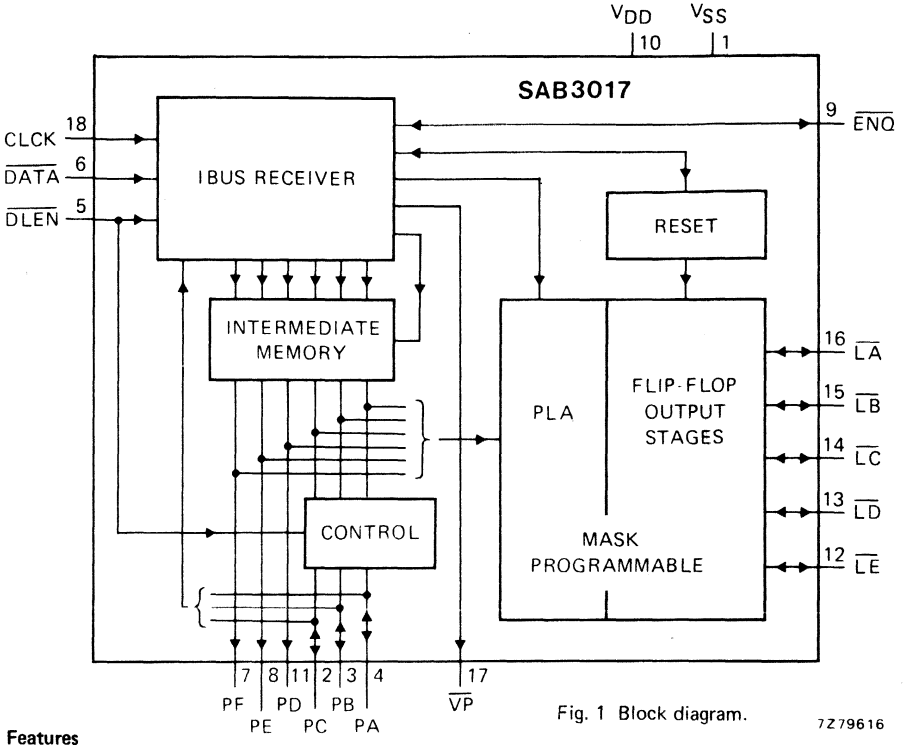


Fig. 1 Block diagram.

7Z79616

Features

- Parallel output (6-bits) of the serial IBUS information for external decoding of 64 commands.
- Five additional outputs can be addressed by internally decoded commands. The selection of these commands is mask-programmable.
- Four different functions can be selected at the decoded outputs: D flip-flop (latch), RS flip-flop, T flip-flop (toggle) or an output pulse.
- It is possible to activate the decoded outputs by presetting each output.
- Eight different preset codes (sub-system addresses) are programmable with external diodes (max. 3 diodes).

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}		0 to +70 °C
Clock frequency	f_{CLCK}	typ.	62,5 kHz
Supply current; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	typ.	14 mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

GENERAL DESCRIPTION

The SAB3017 enables customized systems with parallel inputs to be driven by our remote control system via the serial instruction bus (IBUS), which can be obtained from the remote control receiver circuit (see Fig. 2). Only three signal lines are necessary for the electrical connections to the TV or radio set.

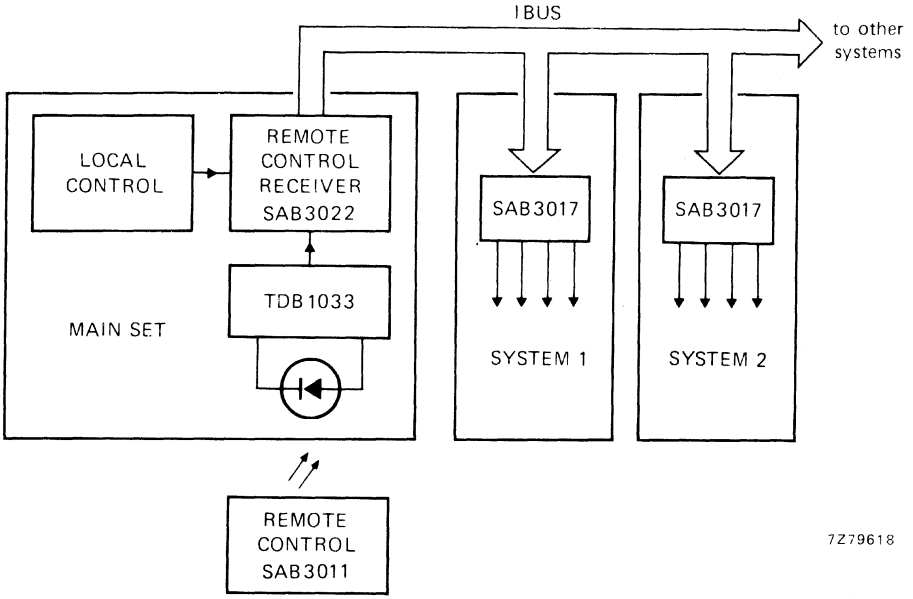


Fig. 2 Customized systems controlled by our remote control system.

The SAB3017 checks the running instruction on the IBUS on format length and transmission errors. This is an important feature, because the signal lines can be used for other data formats. Output $\overline{VP}$ generates a LOW pulse after a valid IBUS transmission. The last valid 6-bit IBUS information is available in parallel at outputs PA to PF; thus up to 64 commands can be decoded by using external logical circuitry.

The SAB3017 also comprises five flip-flop outputs $\overline{LA}$ to $\overline{LE}$, which are mask-programmable. The operation mode of each output is also programmable; D flip-flop (latch), RS flip-flop, T flip-flop (toggle), or a single output pulse are possible. Two internal control signals are available for controlling these functions. The joining of these control signals into a single command or a group of commands is also set by a mask-programmable command decoder. The use of peripheral command decoding is not necessary in simple systems for suitable choice of the functions and the associated commands at these outputs; the SAB3017 can directly take-over the control of these systems.

The system connected to the SAB3017 can be operated by choice, direct or after addressing by a preset code. With the use of external diodes (max. 3 diodes) the circuit is programmable to be addressed by a preset code. One out of eight preset IBUS codes (code no. 56 to 63) can be chosen. The sub-system is only activated when receiving this preset code, e.g. that special sub-system is enabled for reception and transmission of further commands; systems with the other programmed preset codes are disabled simultaneously. All following commands are only executed in the addressed system until a new preset code is received.
Output $\overline{ENQ}$ controls the following circuits of the system; $\overline{ENQ}$ is LOW when the system is enabled and HIGH when disabled. In this way 56 commands are available for controlling the main set and for each sub-system; 8 further commands are reserved for addressing max. 8 sub-systems.

The circuit can also be used without any bus enable addressing. In this case $\overline{ENQ}$ must be connected to a LOW level (ground) and the circuit is always in the enabled state.

OPERATION DESCRIPTION

Inputs (CLCK, $\overline{DLEN}$, $\overline{DATA}$)

The IBUS signals CLCK, $\overline{DLEN}$ and $\overline{DATA}$ are in general common bus-lines for all sub-systems for reception or transmission of commands. The SAB3017 is an IBUS receiving circuit. An IBUS information is transmitted by an IBUS transmitter (e.g. SAB3022) synchronously with the system clock (62,5 kHz) and serially via the $\overline{DATA}$ line; $\overline{DLEN}$ is HIGH during transmission. The timing of the IBUS transmission is shown in Fig. 4.

Outputs (PA, PB, PC, PD, PE, PF and $\overline{VP}$)

The latest IBUS information received is available in parallel at the intermediate memory outputs PA to PF. This is independent of whether the circuit is enabled or not. The terminals PA, PB and PC act as inputs to preset the address (preset code) for this circuit during the IBUS transmission. The preset code for enabling is determined by a connected (0) or not connected (1) diode between the terminals PA, PB, PC and $\overline{DLEN}$ as given in the following table; an example of diode connection is given in Fig. 3.

Table 1. Connection of diodes for the preset codes; 0 = diode, 1 = no diode.

enabling by preset code no.	PC	PB	PA
56	0	0	0
57	0	0	1
58	0	1	0
59	0	1	1
60	1	0	0
61	1	0	1
62	1	1	0
63	1	1	1

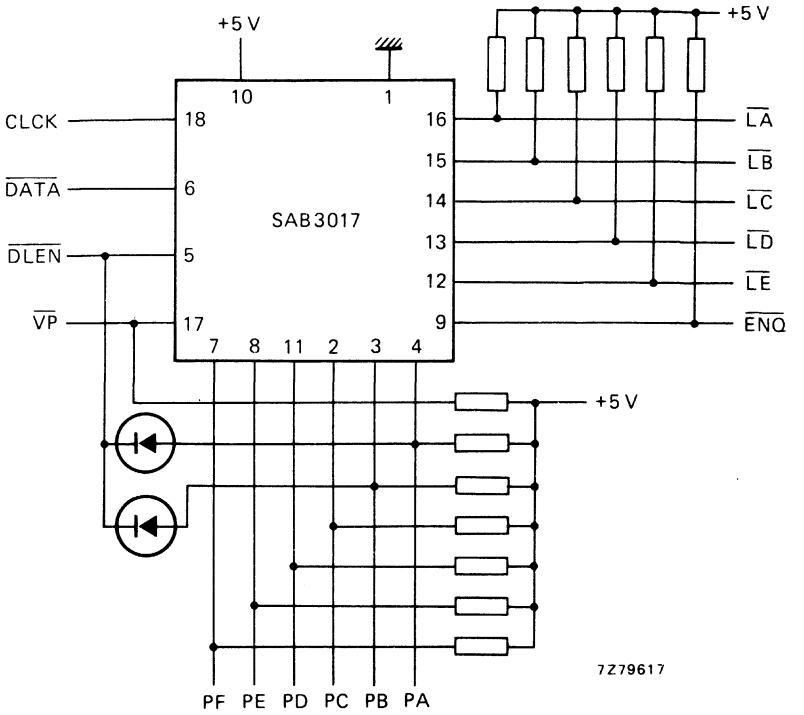


Fig. 3 Example of diode connection for enabling by preset code no 60.

The terminals PA, PB and PC again act as outputs after a valid IBUS transmission. After a pulse at $\overline{VP}$ the new IBUS information is available at the terminals PA to PF untill a new IBUS transmission follows (see Fig. 4). The outputs PA to PF and also $\overline{VP}$ are open drain outputs, so they need external pull-up resistors.

Input/output ($\overline{ENQ}$)

Output $\overline{ENQ}$ = LOW: circuit is enabled; $\overline{ENQ}$ = HIGH: circuit is disabled. The output $\overline{ENQ}$ is enabled after reception of a preset code, which is determined by the diode connection as given in Table 1. It is disabled after reception of one of the other seven preset codes; this is done in case another sub-system is addressed, or after reception of the IBUS code numbers 2 or 4, which are used to address the main set. For timing of $\overline{ENQ}$ see Fig. 4.

Terminal $\overline{ENQ}$ also operates as an input. The circuit is enabled by applying LOW pulses ($T > 2 \times T_{CLCK}$) externally and it is continuously in the enabled state when $\overline{ENQ}$ is connected to ground. Terminal $\overline{ENQ}$ has an open drain output stage, so it needs an external pull-up resistor.

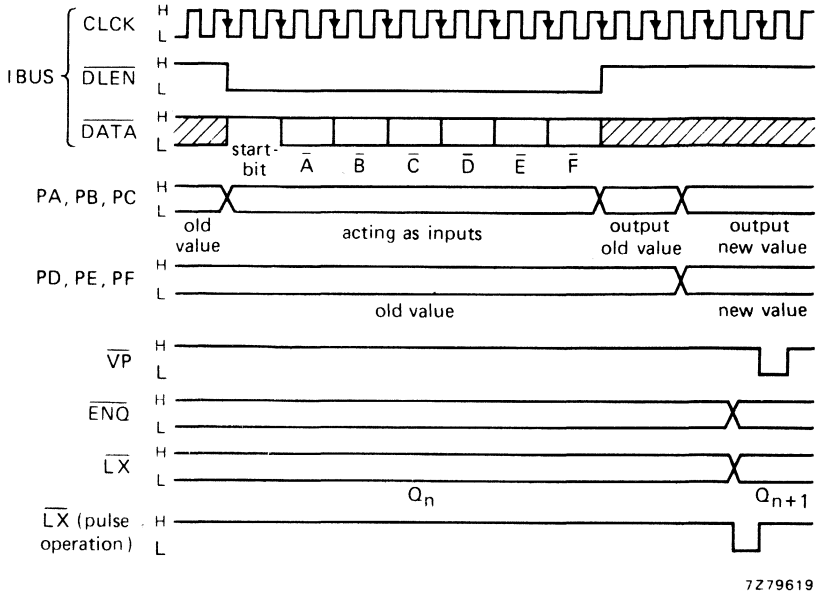


Fig. 4 Timing diagram for the output signals.

Outputs ($\overline{LA}$, $\overline{LB}$, $\overline{LC}$, $\overline{LD}$, $\overline{LE}$)

The operation mode of these outputs is determined by an internal mask-programmable command decoder (see Table 2).
Table 3 shows the mode of the mask-programmed output stages for the standard version SAB3017A.
The signals $\overline{LA}$ to $\overline{LE}$ can only be changed when the circuit is in the enabled state ($\overline{ENQ}$ = LOW). For each single output, the commands x or x and y determine the addressed output.
A group of commands can be specified for x and y, which have a common bit pattern.

The outputs $\overline{LA}$ to $\overline{LE}$ are open drain outputs, so they need external pull-up resistors.

Terminals $\overline{LA}$ to $\overline{LE}$ also operate as inputs: for the functions m = D, T or RS, they can be set LOW by applying a LOW pulse ($T > 2 \times T_{CLCK}$) externally.

Reset

The SAB3017 automatically initiates a reset cycle after switching on the supply. The outputs PA to PF are then LOW; the outputs $\overline{VP}$, $\overline{LA}$ to $\overline{LE}$ and $\overline{ENQ}$ are then HIGH.

Table 2. Possible functions at the outputs $\overline{LA}$ to $\overline{LE}$.

operation mode m	circuit enabled ($\overline{ENQ}$ = 0) output is set (LOW) by	output is reset (HIGH) by	circuit is disabled ($\overline{ENQ}$ = 1)
D = latch	command x	all other commands except x	HIGH
T = toggle	command x	command x	latest state is maintained
RS = set/reset	command x	command y	latest state is maintained
P = pulse	LOW pulse, initiated by command x		HIGH, no pulse

Table 3. Decoded outputs for the standard version SAB3017A.

IBUS code no.	outputs PA to PF						$\overline{LA}$		$\overline{LB}$		$\overline{LC}$		$\overline{LD}$		$\overline{LE}$	
	F	E	D	C	B	A	Q_{n+1}	m	Q_{n+1}	m	Q_{n+1}	m	Q_{n+1}	m	Q_{n+1}	m
14	0	0	1	1	1	0	Q_n		1		Q_n		0	P	1	
15	0	0	1	1	1	1	Q_n		1		Q_n		1		0	P
16	0	1	0	0	0	0	Q_n		1		1	RS	1		1	
17	0	1	0	0	0	1	Q_n		1		1	RS	1		1	
18	0	1	0	0	1	0	Q_n		1		1	RS	1		1	
19	0	1	0	0	1	1	Q_n		1		1	RS	1		1	
20	0	1	0	1	0	0	Q_n		1		1	RS	1		1	
21	0	1	0	1	0	1	Q_n		1		1	RS	1		1	
22	0	1	0	1	1	0	Q_n		1		1	RS	1		1	
23	0	1	0	1	1	1	Q_n		0	D	1	RS	1		1	
32	1	0	0	0	0	0	$\overline{Q}_n$	T	1		Q_n		1		1	
45	1	1	0	1	1	0	Q_n		1		0	RS	1		1	
further	X	X	X	X	X	X	Q_n		1		Q_n		1		1	

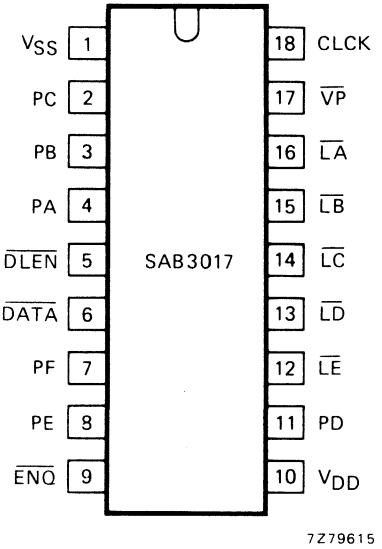


Fig. 5 Pinning diagram.

PINNING

1	V_{SS}	negative supply (0 V)
10	V_{DD}	positive supply
5	$\overline{DLEN}$	data line enable input
6	$\overline{DATA}$	data input
18	CLCK	clock input
4	PA	address inputs
3	PB	address inputs
2	PC	parallel data outputs
11	PD	parallel data outputs
8	PE	parallel data outputs
7	PF	parallel data outputs
16	$\overline{LA}$	decode outputs/set inputs (LOW)
15	$\overline{LB}$	decode outputs/set inputs (LOW)
14	$\overline{LC}$	decode outputs/set inputs (LOW)
13	$\overline{LD}$	decode outputs/set inputs (LOW)
12	$\overline{LE}$	decode outputs/set inputs (LOW)
9	$\overline{ENQ}$	enable input/output
17	$\overline{VP}$	data valid — pulse output

RATINGS (V_{SS} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to +7,5		V
Input voltage range	V_I	−0,3 to +15		V
Output voltage range	V_O	0 to +15		V
Input current	$\pm I_I$	max.	10	mA
Output current	$\pm I_O$	max.	10	mA
Power dissipation per output	P_O	max.	50	mW
Total power dissipation per package	P_{tot}	max.	300	mW
Operating ambient temperature range	T_{amb}	0 to +70		°C
Storage temperature range	T_{stg}	−55 to +150		°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to +70 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	4,5	5	5,5	V	
Supply current	5	I_{DD}	–	14	–	mA	
Input voltage LOW	5	V_{IL}	−0,3	–	1,2	V	
Input voltage HIGH	5	V_{IH}	3,5	–	15	V	
Input leakage current	5	I_{IR}	–	–	1	μA	V_I = −0,3 to +15 V
Output voltage LOW	5	V_{OL}	–	–	1	V	I_O = 1 mA; open drain
Output leakage current	5	I_{OR}	–	–	20	μA	V_O = 15 V (HIGH)
Clock frequency	5	f_{CLCK}	10	62,5	70	kHz	
Input rise/fall times	5	t_r; t_f	–	–	1	μs	

RECEIVER AND ANALOGUE MEMORY

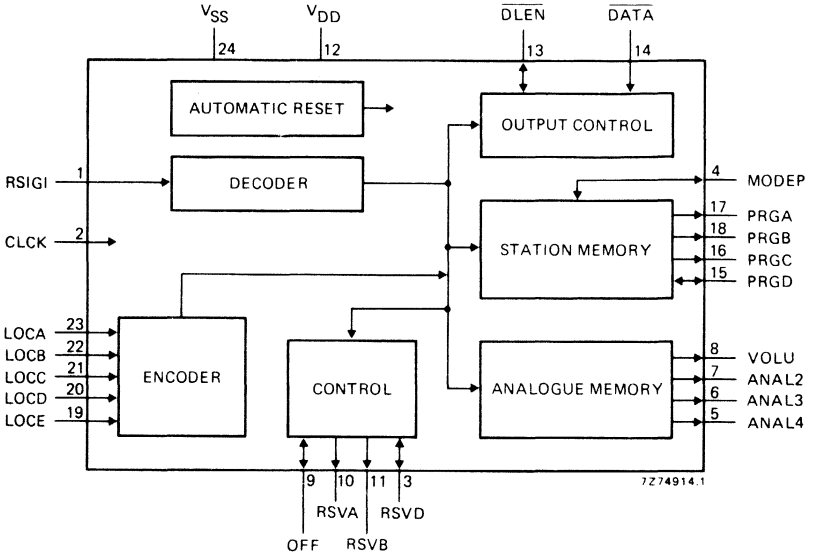


Fig. 1 Block diagram; infrared receiver.

Features

- Receiver for 2 x 64 commands. 6 + 1 bit code word (selectable).
- Four 63-step analogue memories with D/A converter; basic setting 50% (31/64); VOLU 30% (19/64) or 50% (31/64).
- Short response time (speed for altering the analogue memories): 115 ms/step; 7,3 s/63 steps.
- ON/OFF (standby) output.
- Serial instruction output (IBUS).
- High security against interference.
- The output signals of the station memory and the IBUS commands are available simultaneously.
- Inputs for local operation via diode-encoded keys; up to 31 commands; mask-programmable.
- Various repetition rates at the IBUS for single commands, step commands (2/second) and analogue commands (8/second).
- Outputs for sub-systems.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ. 5 V
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Clock frequency	f_{CLCK}	62,5 kHz
Supply current at V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	typ. 20 mA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The circuit is implemented in N-channel MOS technology. Serial data is derived from the transmitter SAB3011 in remote or extended local operation mode. This data is applied to the RSIGI input, where it is checked and decoded and serially applied as commands to the IBUS. Some commands are also used internally for control of 4 analogue functions and the station memory. Moreover, the circuit has available an input/output for the ON/OFF function, three auxiliary outputs for reserve commands, each containing the station-change signal and a sub-system identification signal. For local operation, five inputs are available, via which 31 different commands are parallel addressable (can be chosen by mask-programming).

Special features:

- Serial output for 64 commands.
- Universal control functions for sub-systems, e.g. tuning systems, Teletext, Viewdata, videogames, clock with addressable memory, etc.
- After addressing a sub-system, the analogue functions and the reserve functions remain available.
- Parallel station outputs.

OPERATION DESCRIPTION

Remote control data input (RSIGI)

Serial data is derived from the transmitter in remote or local operation mode. This data is applied to the RSIGI input (see Fig. 2), where it is checked and decoded. The instruction bus (IBUS) is then enabled and an output operation takes place.

Response time for infrared operation: ≈ 110 ms.

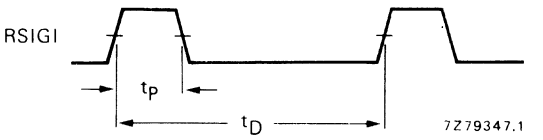
The following tests are carried out for each signal or signal group:

- Dead-time, (time between two pulses).
- Word separation.
- Bit counting.
- Word comparison.

Signals which do not come within the zero or one 'window', restart the input detection procedure. The commands are transmitted as 7-bit words (1 start bit, 6 data bits). The system will accept leading '0' command (start bit S = 0) for RSVD = HIGH and leading '1' commands (S = 1) for RSVD = LOW.

Table 1 shows the IBUS-codes.

zero time (t_D)	one time (t_D)	infrared operation mode
5,1 ms ± 1 ms	7,2 ms ± 1 ms	IRA (wide window)
5,1 ms ± 0,13 ms	7,2 ms ± 0,13 ms	IRB (narrow window)

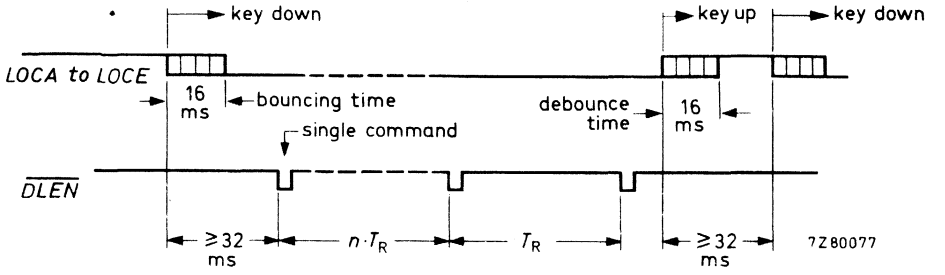


t_P = 1,1 ms

Fig. 2 Specification of the timing of the input signal.

Local keyboard inputs (LOCA, LOCB, LOCC, LOCD and LOCE)

Up to 31 commands (see Table 2) for local control are possible by addressing these 5 inputs from a binary encoded keyboard. The inputs are drawn internally to V_{DD} at standby. Out of the 64 commands 31 can be stored in the mask-programmable ROM with the desired key addresses. This ROM can be chosen by the user. The ROM of the standard version SAB3022B (see Table 2) is programmed by the manufacturer. A keyboard input (local control) overrides the remote control commands at input RSIGI (from SAB3011). Current IBUS output data is completely stopped.



Repetition rate: 2/second x T_R = 516 ms
8/second x T_R = 129 ms

Fig. 3 Relationship between key operation and command output.

Table 1. Specifications of the IBUS-code (continued on next page).

RSIGI/ IBUS code no.	instruction code F	E	D	C	B	A	function	CL.*	OFF	RSVA	RSVB	VOLU	ANAL2	ANAL3	ANAL4	RSVD	MODEP	PRCA	PRCB	PRCC	PRCD
0	0	0	0	0	0	0	basic set analogue	S				**	31/64	31/64	31/64						
1				0	0	1	mute/on	S	0			0									
2				0	1	0	OFF	S	1								1				
3				0	1	1	reserve A	S		0/1											
4				1	0	0	on	R8	0								1				
5				1	0	1	on	S	0												
6				1	1	0	reserve B/on	S	0		⊓⊓										
7				1	1	1	reserve C/on	S	0		⊓⊓										
8	0	0	1	0	0	0	reserve D▲	R8								⊔					
9				0	0	1	–	R8													
10				0	1	0	–	R8													
11				0	1	1	–	R8													
12				1	0	0	–	R8													
13				1	0	1	–	R8													
14				1	1	0	–	R8													
15				1	1	1	–	R8													
16	0	1	0	0	0	0	on/station 16	S	0			⊔				⊔		1	1	1	1
17				0	0	1	on/ 1	S	0			⊔				⊔		0	0	0	0
18				0	1	0	on/ 2	S	0			⊔				⊔		1	0	0	0
19				0	1	1	on/ 3	S	0			⊔				⊔		0	1	0	0
20				1	0	0	on/ 4	S	0			⊔				⊔		1	1	0	0
21				1	0	1	on/ 5	S	0			⊔				⊔		0	0	1	0
22				1	1	0	on/ 6	S	0			⊔				⊔		1	0	1	0
23				1	1	1	on/ 7	S	0			⊔				⊔		0	1	1	0
24	0	1	1	0	0	0	on/ 8	S	0			⊔				⊔		1	1	1	0
25				0	0	1	on/ 9	S	0			⊔				⊔		0	0	0	1
26				0	1	0	on/ 10	S	0			⊔				⊔		1	0	0	1
27				0	1	1	on/ 11	S	0			⊔				⊔		0	1	0	1
28				1	0	0	on/ 12	S	0			⊔				⊔		1	1	0	1
29				1	0	1	on/ 13	S	0			⊔				⊔		0	0	1	1
30				1	1	0	on/ 14	S	0			⊔				⊔		1	0	1	1

32	1	0	0	0	0	0	–		S	–														
33				0	0	1	–		S															
34				0	1	0	on		S	0														
35				0	1	1	on		S	0														
36				1	0	0	on/step station up		R2	0			⊔					⊔		X	X	X	X	
37				1	0	1	on/step station down		R2	0			⊔					⊔		X	X	X	X	
38				1	1	0	on		R2	0														
39				1	1	1	on		R2	0														
40	1	0	1	0	0	0	volume up		R8				→1											
41				0	0	1	volume down		R8				→0											
42				0	1	0	ANAL2 up		R8					→1										
43				0	1	1	ANAL2 down		R8					→0										
44				1	0	0	ANAL3 up		R8						→1									
45				1	0	1	ANAL3 down		R8						→0									
46				1	1	0	ANAL4 up		R8							→1								
47				1	1	1	ANAL4 down		R8							→0								
48	1	1	0	0	0	0	–		S															
49				0	0	1	–		S															
50				0	1	0	–		S															
51				0	1	1	on		S	0														
52				1	0	0	on		R8	0														
53				1	0	1	on		R8	0														
54				1	1	0	on		R8	0														
55				1	1	1	on		R8	0														
56	1	1	1	0	0	0	on		R8	0									0					
57				0	0	1	on		R8	0									0					
58				0	1	0	on		R8	0									0					
59				0	1	1	on	station memory	R8	0									0					
60				1	0	0	on	disconnected	R8	0									0					
61				1	0	1	on		R8	0									0					
62				1	1	0	on		R8	0									0					
63				1	1	1	on		R8	0									0					

* Instruction class (CL.): S = single
R2 = repeat ≈ 2/second
R8 = repeat ≈ 8/second

** Mask-programmed; 19/16, 31/64 or unchanged.

▲ MODEP = LOW.

⊔: mute control

X : change of station counter

Table 2. Allocation of local command codes for the standard version (SAB3022B).

IBUS code no.	local control inputs					command valid for DICS system
	LOCE	LOCD	LOCC	LOCB	LOCA	
	1	1	1	1	1	no command
36	1	1	1	1	0	step station up
33	1	1	1	0	1	store
1	1	1	1	0	0	mute
5	1	1	0	1	1	search up/on
38	1	1	0	1	0	step channel up
40	1	1	0	0	1	volume up
41	1	1	0	0	0	volume down
4	1	0	1	1	1	display short
32	1	0	1	1	0	display on/off
42	1	0	1	0	1	ANAL 2 up
43	1	0	1	0	0	ANAL 2 down
44	1	0	0	1	1	ANAL 3 up
45	1	0	0	1	0	ANAL 3 down
39	1	0	0	0	1	step channel down
34	1	0	0	0	0	channel mode
37	0	1	1	1	1	step station down
2	0	1	1	1	0	OFF
48	0	1	1	0	1	–
49	0	1	1	0	0	–
46	0	1	0	1	1	ANAL 4 up
47	0	1	0	1	0	ANAL 4 down
50	0	1	0	0	1	–
56	0	1	0	0	0	reserved
0	0	0	1	1	1	basic set analogue
6	0	0	1	1	0	reserve B
7	0	0	1	0	1	reserve C
57	0	0	1	0	0	reserved
58	0	0	0	1	1	reserved
17	0	0	0	1	0	station 1
35	0	0	0	0	1	search down
59	0	0	0	0	0	reserved

IBUS outputs

Outputs $\overline{DATA}$ and $\overline{DLEN}$ are inverted.

Correctly received commands are available for the duration of a key operation as a single command or as repeated commands, in accordance with the sub-system requirements (see Table 1). The following output modes are provided:

- Single command; e.g. digits.
- Repetition rate: 2/second; e.g. step functions.
- Repetition rate: 8/second; e.g. analogue functions.

The IBUS command is available at output $\overline{DATA}$ synchronous with the system clock; the word length is 7 bits, one start bit and 6 data bits.

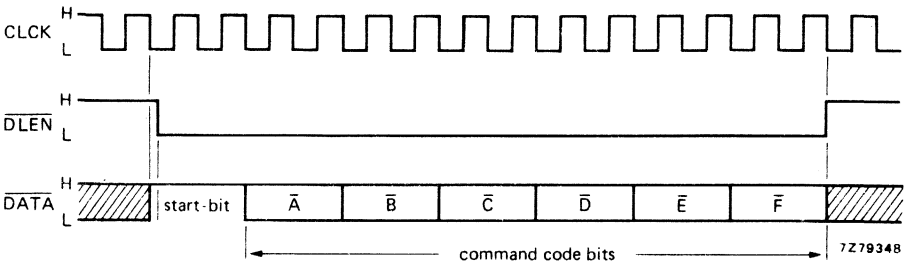


Fig. 4 Output waveforms of a command transmission.

Various word formats can be transmitted between the sub-systems, so it is necessary that each receiver should carry out recognition of a word format. Word formats which do not correspond with the requirements have no effect on the system. It is also necessary that all sub-systems which receive or supply information to the BUS-line should check whether or not the BUS is occupied, if yes, the output is delayed. Output $\overline{DLEN}$ acts as an input for this procedure. The output delay amounts to $32 \times t_{CLCK} = 512\ \mu s$.

Analogue memories

The SAB3022 contains four 64-step memories for analogue functions. The speed of stepping is 115 ms/step.

Stepping through the full range takes: 7,3 seconds.

When operating in the local mode, via inputs LOCA to LOCE, the stepping speed becomes 129 ms/step; 8,2 seconds for the full range.

The output waveform of the analogue values is pulse-width modulated and has a repetition rate of approximately 2 kHz; the duty factor determines the analogue values. The analogue voltage is available at the output of an externally connected low-pass filter.

By the command (0) 'basic setting' and after switching-on the supply, the analogue memories (ANAL 2, ANAL 3 and ANAL 4) are preset to a mid-position (31/64 in the standard version). The VOLU memory is set to 30% in the standard version, after switching-on the supply (set to 50% and/or set to normal by command 0 can be obtained by mask-programming).

The volume control output (VOLU) is set LOW when, by a mute command (1), the flip-flop is set. The volume output will be set LOW for T_S = 200 ms (see Fig. 5) when the station is changed by the following commands (only if MODEP = HIGH):

16 to 31 (station 1 to 16).
36 and 37 (step station up/down).

The flip-flop will be reset by the following commands:

mute command (1).
volume up command (40); the volume output increases from LOW.
basic setting command (0); if chosen by mask-programming.
OFF command (2).

In the standby mode, output OFF = HIGH, the analogue memories cannot be changed. The output VOLU = LOW, independent of memory values.

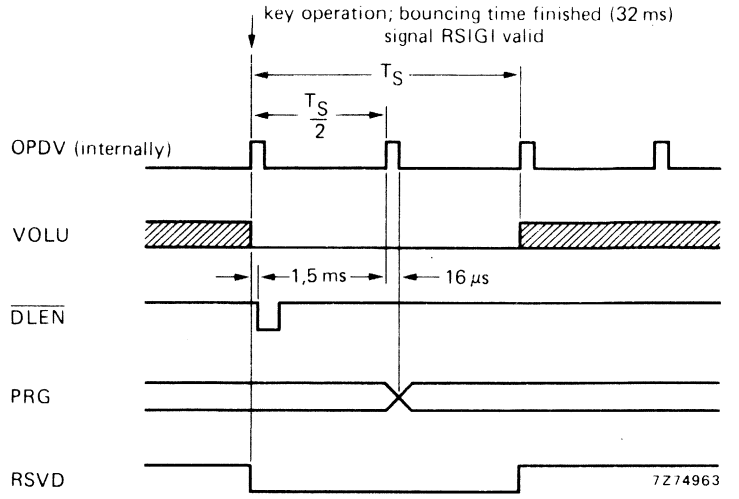


Fig. 5 Timing diagram for muting at station and channel selection.

RSIGI mode (from SAB3011)	T_S
infrared transmission	200 ms
local operation	260 ms

Input/output OFF

OFF is the output of a flip-flop (ON/OFF-flag). If this output is LOW, the system is in the ON-mode, if HIGH, the system is in the standby mode. The system is set to the standby mode by switching on the supply or using the command OFF. Terminal OFF operates as an input and allows setting of the flip-flop to the on-state e.g. switching on via a wiping contact on the mains switch, while OFF is forced to V_{SS} for at least two clock cycles. The flip-flop can be set LOW = ON by a number of commands (see Table 1).

Reserve outputs (RSVA, RSVB and RSVD)

RSVA is the output of a flip-flop which changes its state after each RESERVE A command (3).

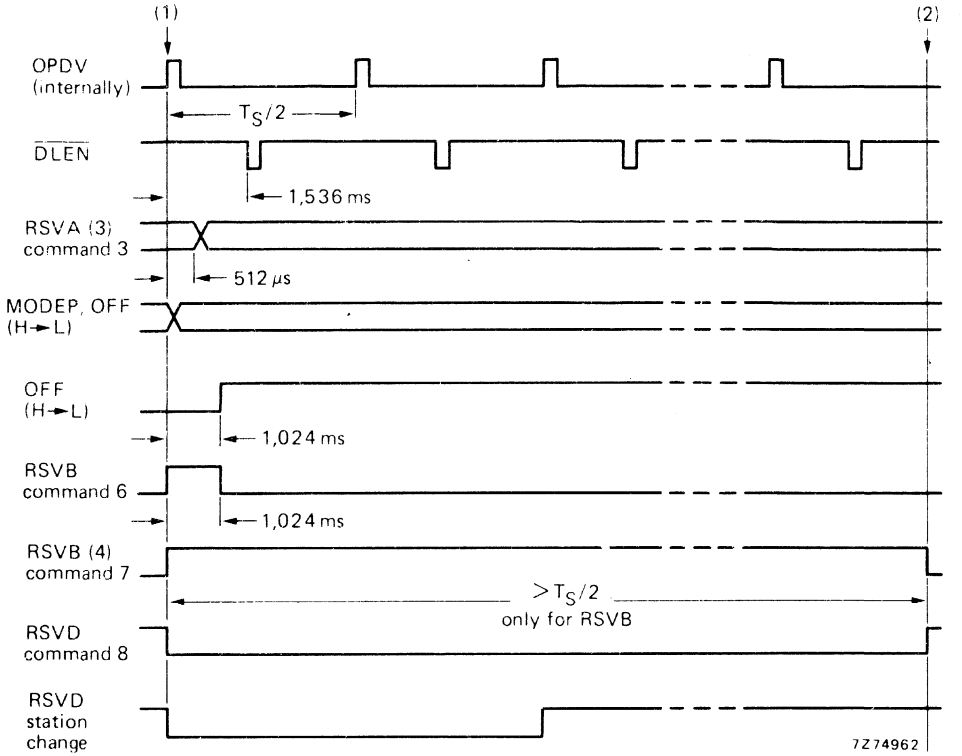
RSVB provides a single positive pulse for 1 ms upon receipt of a RESERVE B command (6).

A RESERVE C command (7) generates a HIGH level on the RSVB output for as long as the command is received, with a minimum of 100 ms (error-free reception assumed).

The function of the RSVD output depends upon the use of the MODEP output. If MODEP is LOW, the RSVD output is LOW as long as the RESERVE D command (8) is received, with a minimum of 100 ms.

If MODEP = HIGH, a LOW pulse appears on the RSVD output during a change of the station memory contents by the commands 16 to 31, 36 and 37 (see also Figs 5 and 6).

RSVD can also be used as an input: if it is connected to ground (V_{SS}), the circuit will expect to receive remote commands with a leading one in place of a leading zero.



(1) Key down; bouncing time finished; signal RSIGI: word comparison effective.

(2) Key up; bouncing time finished; signal RSIGI: word comparison uneffective, or the time-window has been exceeded.

(3) For SAB3032: RSVF, command 10.

(4) For SAB3032: RSVE, command 9.

Fig. 6 Timing diagram for some outputs; f_{CLCK} = 62,5 kHz.

Station memory outputs (PRGA, PRGB, PRGC, PRGD and MODEP)

The station memory outputs are coded as shown in Table 1.

These are the outputs of a 4-bit station memory, the content of which is changed by commands 16 to 31 (station 1 to 16) or commands 36 and 37 (step station up/down). A step station command (36 and 37) in the standby mode switches the system into the ON-mode without station alteration.

The MODEP terminal indicates whether a sub-system is selected (MODEP = LOW) or not (MODEP = HIGH). A sub-system is selected by the commands 56 to 63. When a sub-system is selected, or when MODEP is switched LOW externally, the commands 16 to 31, 36 and 37 do not influence the station memory contents. Output VOLU is not mute controlled and RSVD delivers no station change signal, and can only be influenced by command 8 (reserve D).

At commands 2 (OFF), 4 (on) and after switching on the supply voltage, the circuit is in the MODEP = HIGH state, meaning the station memory can be addressed.

When the SAB3022 is used in the DICS (Digital Channel Selection) system, MODEP should be switched LOW externally, to avoid unwanted muting during input of digits.

The step station cycle is reduced from 16 to 12 stations, if PRGD is connected to ground (V_{SS}).

Standby state

The SAB3022 has a built-in reset circuit. After switching on the supply voltage, the next two clock cycles will reset the circuit into the standby mode.
The circuit will be in the following operating states:

1. VOLU = LOW.
2. Analogue memories are set to 50%; VOLU is set to 30% (for the standard version).
3. Station memory is at station 1.
4. OFF = HIGH.
5. Mute-flag is not set.
6. All reserve outputs (except RSVD) are LOW.
7. MODEP = HIGH.

Programming of modes using outputs as inputs

Several outputs can be used as inputs (MODEP, RSVD, PRGD), for programming other operating modes. This can be obtained in 2 ways:

1. By means of a connection to ground (V_{SS}). In this case the output signal is not available.
2. By means of a bipolar transistor in a common emitter circuit which clamps the output level at V_{BE} (see Fig. 6). The output signal is available with reversed polarity at the collector of the transistor.

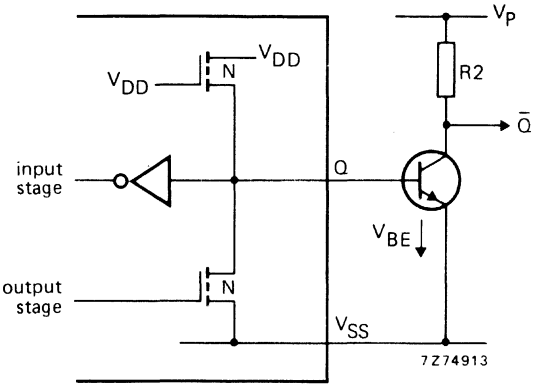


Fig. 6 Clamping the output voltage to V_{BE}.

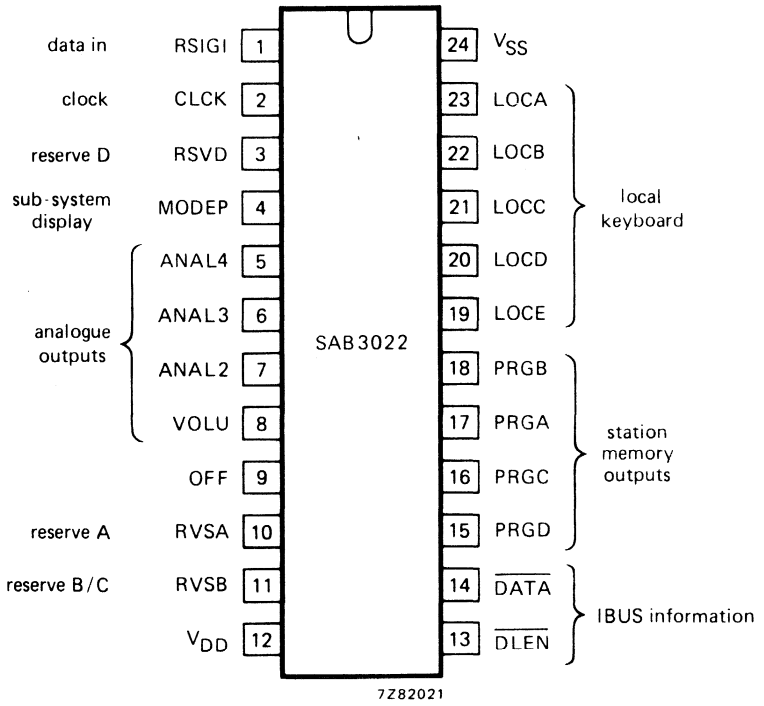


Fig. 7 Pinning diagram.

RATINGS (V_{SS} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	max.	7,5 V
Input voltage	V_I	max.	15 V
Input current	I_I	max.	10 mA
Negative input current	$-I_I$	max.	10 mA
Output current	I_O	max.	10 mA
Negative output current	$-I_O$	max.	10 mA
Power dissipation per output	P_O	max.	50 mW
Total power dissipation per package	P_{tot}	max.	500 mW
Operating ambient temperature range	T_{amb}		−20 to + 70 °C
Storage temperature range	T_{stg}		−55 to + 150 °C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	4,5	5,0	5,5	V	
Supply current	5	I_{DD}	–	–	25	mA	
Input voltage LOW	5	V_{IL}	–0,3	–	1,2	V	
Input voltage HIGH	5	V_{IH}	3,5	–	15	V	
Input leakage current RSIGI, CLCK	5	I_{IR}	–	–	1	μA	V_I = –0,3 to + 10 V
Input current LOW LOCA to LOCE, OFF, $\overline{DLEN}$	5	$-I_{IL}$	–	–	100	μA	V_I = 0
Outputs OFF, RSVA, RSVB, RSVD, MODEP, PRGA to PRGD							
Output voltage LOW	5	V_{QL}	–	–	0,8	V	I_{QL} = 1 mA
Output current HIGH	5	I_{QH}	–	–	20	μA	V_{QH} = 15 V
Outputs $\overline{DATA}$, $\overline{DLEN}$							
Output voltage LOW	5	V_{QL}	–	–	0,8	V	I_{QL} = 2 mA
Output current HIGH	5	I_{QH}	–	–	20	μA	V_{QH} = 15 V
Outputs VOLU, ANAL2 ANAL3, ANAL4							
Output voltage LOW	5	V_{QL}	–	–	1	V	I_{QL} = 4 mA
Output current HIGH	5	I_{QH}	–	–	20	μA	V_{QH} = 15 V
Outputs RSVA, RSVD, MODEP, OFF, PRGD							
Output voltage HIGH	5	V_{QH}	3,5	–	15	V	$I_Q > 0$
Input OFF current during standby setting	5	I_{OFF}	15	–	–	mA	$V_{QL} \rightarrow V_{QH}$
Clock frequency	5	f_{CLCK}	56,25	62,5	68,75	kHz	
Duty factor	5	δ	0,4	0,5	0,6		
Input rise/fall time	5	t_r; t_f	–	–	1	μs	

APPLICATION INFORMATION

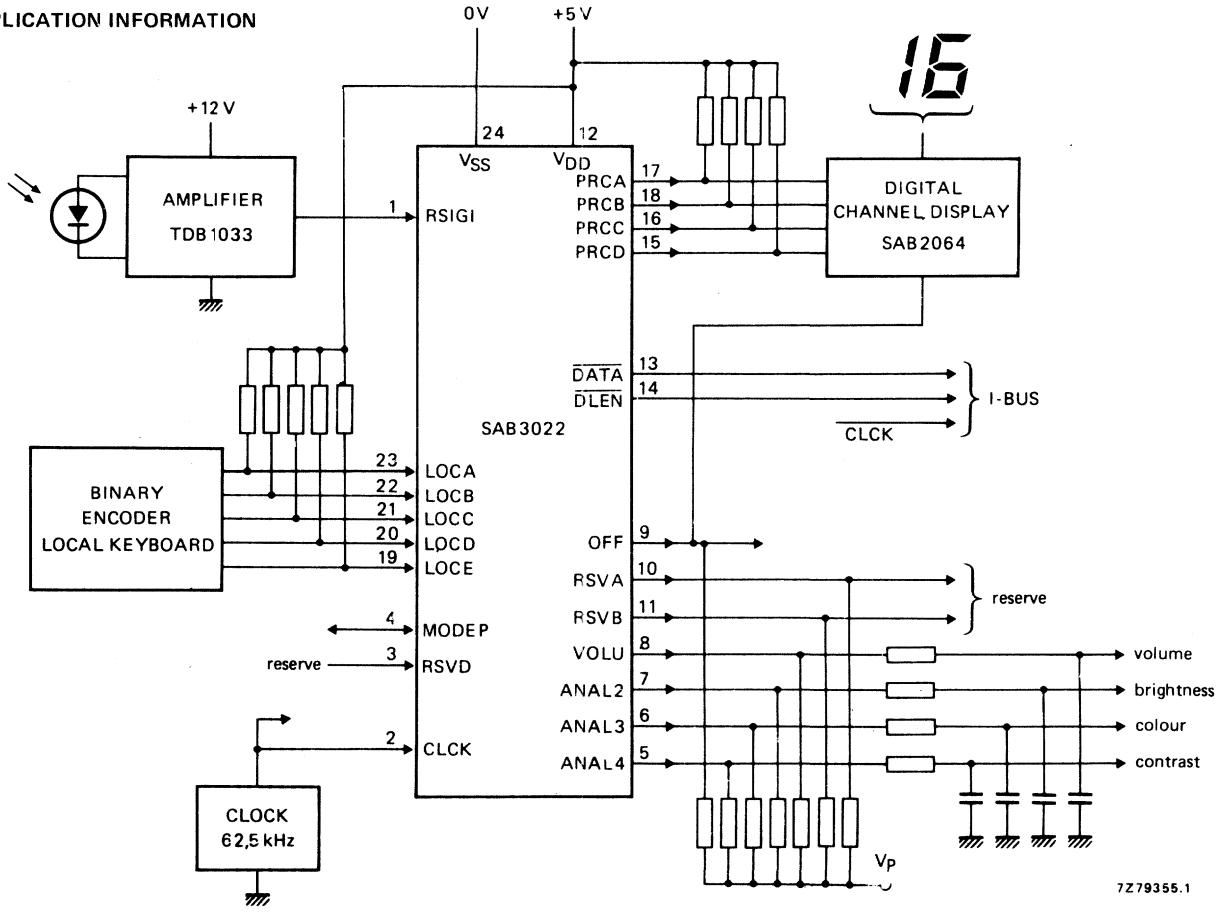


Fig. 8 Typical receiver circuit using SAB3022.

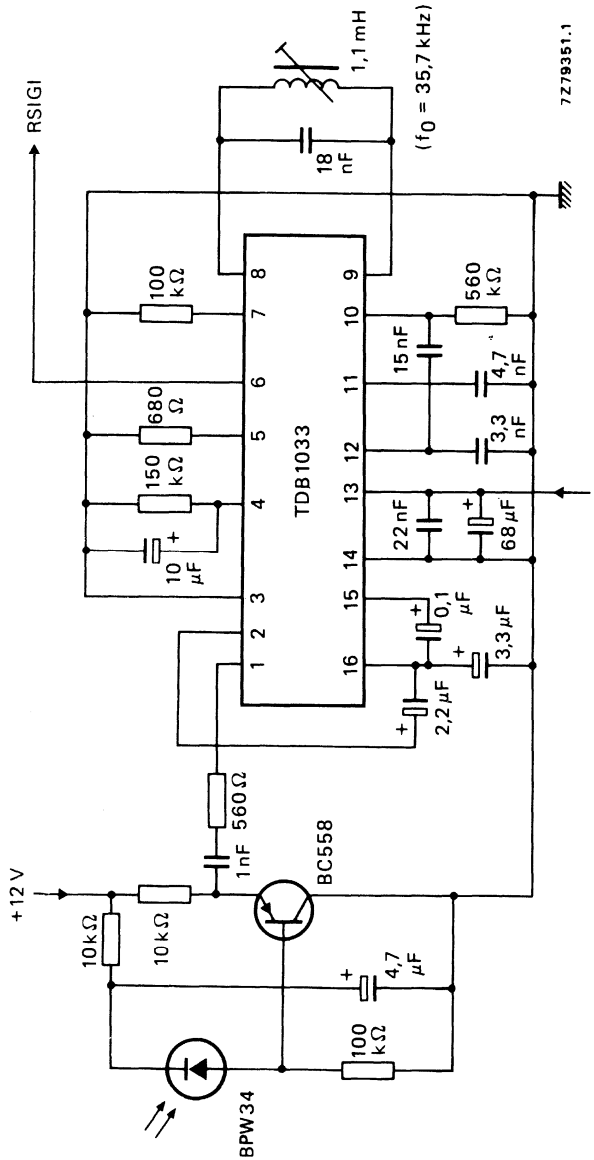


Fig. 9 Circuit diagram of infrared detector and amplifier.

COMPUTER INTERFACE FOR TUNING SYSTEMS (CITUS)

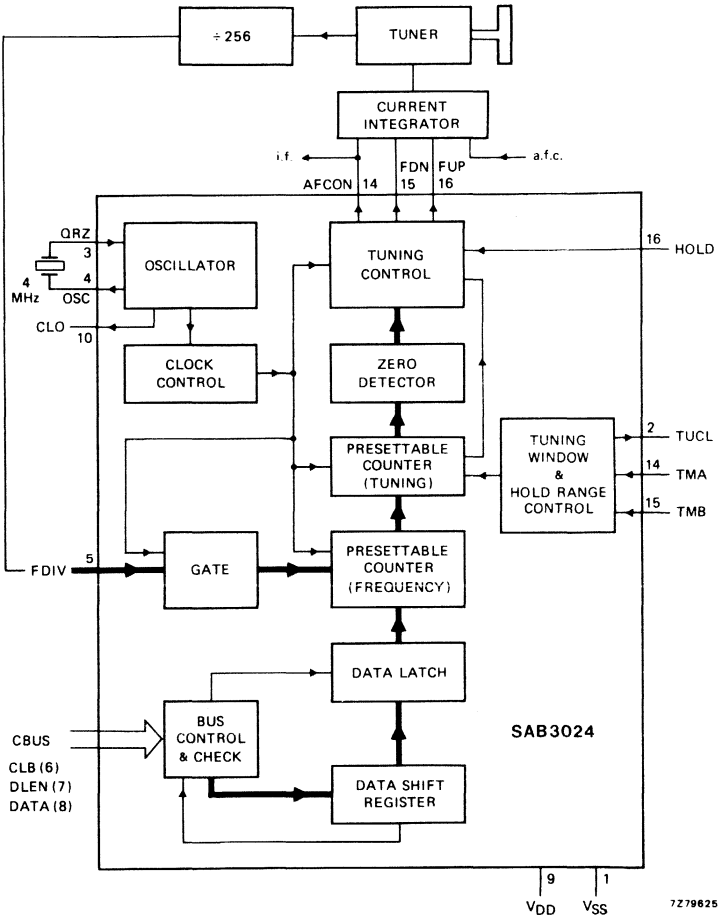


Fig. 1 Block diagram.

The circuit comprises the following:

- CBUS receiver with an 18-bit shift register, BUS control, an 18-bit latch for storing the frequency information.
- A 14-bit presettable frequency counter to measure the incoming frequency at FDIV.
- Tuning control with tuning counter; zero detection; control of tuning windows and hold ranges.
- An on-chip crystal oscillator and power on reset.
- A.F.C. is not necessary because of the accuracy of 62,5 kHz for the frequency measurement.

PACKAGE OUTLINE 16-lead DIL; plastic (SOT-38Z).

GENERAL DESCRIPTION

The SAB3024 accepts commands from the microcomputer via the CBUS and performs the functions associated with frequency-locked loop digital tuning. Receiver tuning data is transmitted from the microcomputer, via the CBUS, as 18-bit words which are loaded into the data shift register. Shortly after the end of each word, the data, if valid, is loaded into the data latch.
The 14 most significant bits of the data word define the required frequency and are loaded into the frequency counter. The cycles of the tuner local oscillator waveform (divided by 256) at the FDIV input then decrement the frequency counter during a 4096 μs measuring period. The content of the frequency counter at the end of this period defines the tuning error as follows:
– counter has passed zero: frequency too high,
– counter has not reached zero: frequency too low,
– counter contents zero: frequency correct.

The remaining content of the frequency counter is loaded into the tuning counter which is decremented to zero. The period during which the tuning counter runs is therefore proportional to the extent of the necessary frequency correction. The tuning control, in conjunction with an external circuit, generates FUP (increase frequency) or FDN (decrease frequency) pulses with a duration equal to the running time of the tuning counter. If the counter content was zero, neither FUP or FDN pulses are generated but the AFCON output is set HIGH to switch on the a.f.c. to the tuner, thereby allowing the tuning operation to be completed. Since the frequency is measured by a 14-bit counter, the maximum tuning error is $f/2^{14}$. With an upper frequency limit of 1024 MHz, this results in a maximum tuning error of 62,5 kHz. This tuning window is narrow enough to allow the system to be used in television receivers that do not incorporate a.f.c. The AFCON output can then be used to control a correct tuning indicator. If a.f.c. is used, it will remain switched on by the AFCON signal as long as the tuning remains within a holding range of 62,5 kHz. Inputs TMA and TMB can also be addressed to give tuning windows of 250 kHz, 500 kHz or 1 MHz and corresponding holding ranges of 500 kHz, 1 MHz or 2 MHz by reducing the length of the frequency counter to 12, 11 or 10 bits.
Two bits of the data word define the rate at which the tuning counter is decremented and thereby control the duration of the FDN and FUP frequency correction pulses. Four durations can be selected for each tuning window width so that the characteristics of various tuners can be accommodated.
Two other bits of the data word can be used to reverse the tuning direction information applied to the tuning control. This facility is included because, if the tuner local oscillator ceases to function, the divide by 256 prescaler may oscillate at high frequency. In this event, the tuning loop will sense that the measured frequency is too high and will be unable to tune up. To overcome this condition, the FDN pulses must be changed to FUP pulses.
A HIGH level at the HOLD input will inhibit the tuning pulses and cause the AFCON output state to remain unchanged.

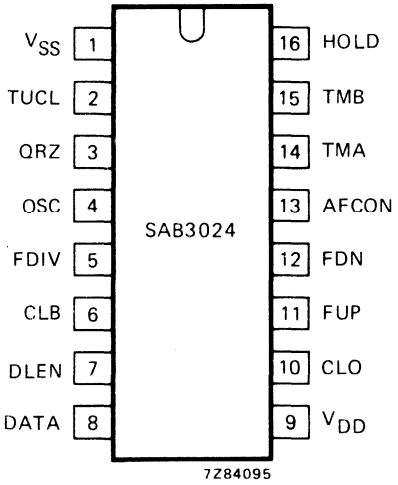


Fig. 2 Pinning diagram.

RECEIVER AND ANALOGUE MEMORY

The SAB3032 is identical to the SAB3022 except for extra output functions; ANDA, **ANDB**, RSVE, RSVF.

Additional features

- Output of a binary-coded display command to realize on-screen bar display or digit display of the stored analogue values.
- Output of a control command for the display of analogue values.
- Two extra reserve functions.

GENERAL DESCRIPTION

With the SAB3032 the following display possibilities can be obtained in addition to the SAB3022.

- On-screen bar display with different colours for each analogue function.
- Multiple on-screen bar display of all analogue functions.
- Numerical display of the altered analogue functions.
- Multiple numerical display of the analogue values.

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Clock frequency	f_{CLCK}		62,5 kHz
Supply current at V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	typ.	20 mA

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

OPERATION DESCRIPTION

Reserve outputs (RSVE, RSVF)

A reserve E (9) command generates a HIGH level on the RSVE output for as long as the command is received at the remote control or at the receiver.
RSVF is the output of a flip-flop which changes its state after each reserve F (10) command. After switching on the supply voltage output RSVF = LOW.
Fig. 6 of the SAB3022 shows the timing of these outputs (see data sheet SAB3022).

Display of analogue values outputs (ANDA, ANDB)

Output ANDA generates a clock and a gating signal synchronized with the IBUS output (see Fig. 1). The addressed analogue values (VOLU, ANAL2, ANAL3, ANAL4) are generated by the clock signal together with the $\overline{\text{DATA}}$ signal, which are available at output ANDB in binary code.
When the analogue value is changed by a command, the specific binary-coded analogue value will be generated serially (simultaneously with the gating signal at ANDA). The signal of the addressed analogue value is generated at ANDB simultaneously. This output is obtained at every analogue value change, thus also at the commands basic set analogue mute/on and OFF, and after switching on the supply voltage.
When no special analogue function is selected the output VOLU is switched to ANDB.
When ANDB is connected to V_{SS}, analogue memory output VOLU will be affected by the command basic set analogue (0).

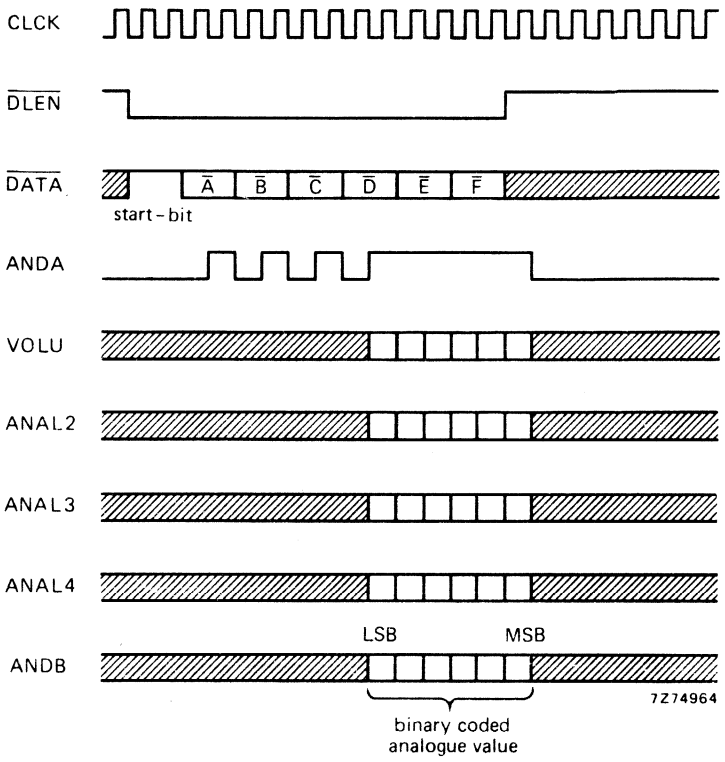


Fig. 1 Timing diagram for signals ANDA and ANDB; display of analogue value.

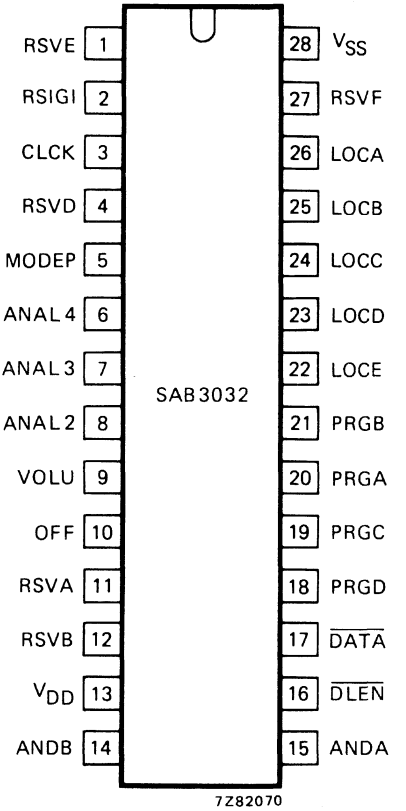


Fig. 2 Pinning diagram; based on development samples, may be changed in future designs.

RATINGS see SAB3022

CHARACTERISTICS see SAB3022 except for:

V_{SS} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Outputs RSVE, RSVF, ANDA, ANDB							
Output voltage LOW	5	V_{QL}	–	–	0,8	V	I_{QL} = 1 mA
Output current HIGH	5	I_{QH}	–	–	20	μA	V_{QH} = 15 V

ANALOGUE AND TUNING CIRCUIT (A & T)

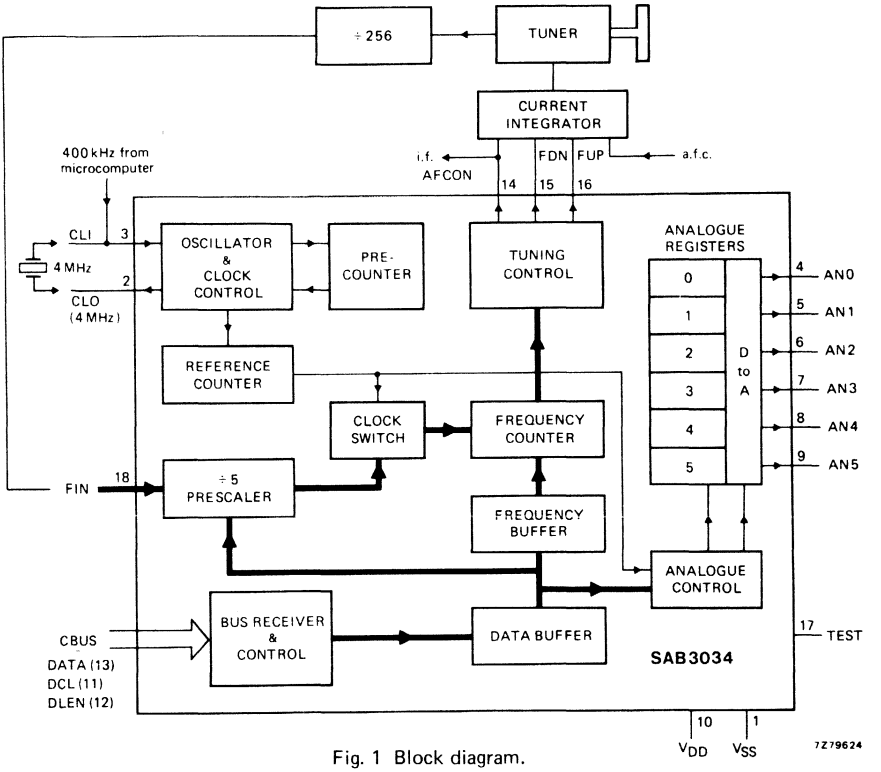


Fig. 1 Block diagram.

The SAB3034 analogue and tuning circuit (A & T) provides closed loop digital tuning and control of up to six analogue functions. The IC is used in combination with a microcomputer and comprises the following:

- Frequency measurement.
- Digital to analogue conversion of 6 analogue functions.
- Command data handling.
- Tuning control.
- Although an on-chip 4 MHz crystal oscillator is provided, the 400 kHz clock output of the microcomputer can directly be used (see Fig. 1 pins 2 and 3).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

GENERAL DESCRIPTION

The SAB3034 performs frequency-locked loop digital tuning and also provides digital control of up to six analogue functions. Control data is transmitted from a microcomputer, via the CBUS (inputs DATA, DLEN and DCL) as sixteen 12-bit words.
Serial data on input DATA is shifted into the data receiver with the data clock DCL, when the data line enable signal DLEN is HIGH. Valid received data is loaded into the data buffer.
Six words define the tuning window, the holding range, the tuning speed and the clock oscillator frequency.
The clock frequency of 400 kHz may be derived directly from a microcomputer or may be generated with a 4 MHz crystal-controlled oscillator. Eight data words control the analogue part. Two data words provide 12 bits of frequency data.

The 12-bit frequency counter has an accuracy of 1024 MHz/2^{12} = 250 kHz which is within the catching range of a.f.c. circuits. With one frequency defining word, frequencies up to 2^{10} MHz = 1024 MHz can be specified in increments of 1 MHz.
While with a second data word increments of 250 kHz in frequency can be specified.
Six data words set the required values (0 to 63) into the six 6-bit analogue registers. The contents of the registers are converted into pulse-width modulated outputs with a frequency of 6,25 kHz and a duty factor proportional to the analogue value (see Fig. 2).
External RC filters smooth the analogue outputs to obtain d.c. control voltages for the ICs in the television receiver. Two data words simultaneously enable or disable all of the analogue outputs.

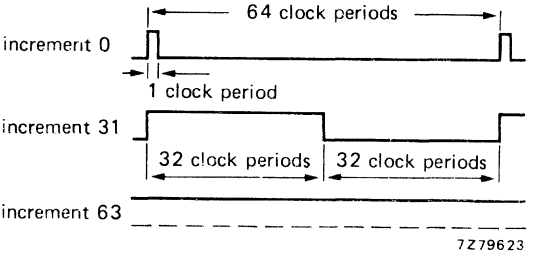


Fig. 2 Pulse-width modulated analogue outputs from the SAB3034.

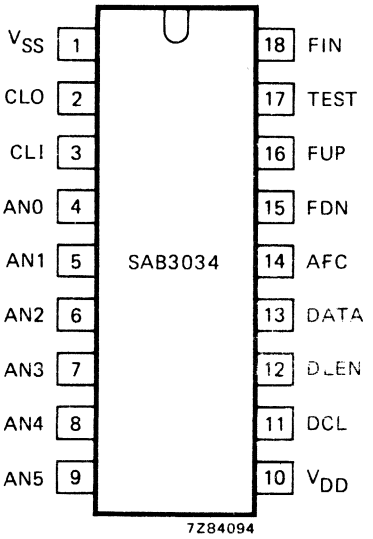


Fig. 3 Pinning diagram.

INFRARED DECODER; MICROCOMPUTER COMPATIBLE

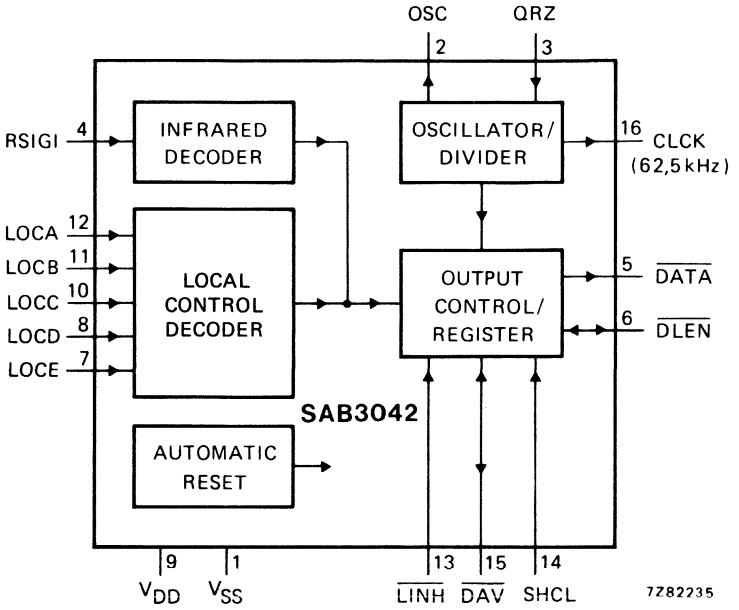


Fig. 1 Block diagram.

Features

- Remote control receiver for 128 commands to be used in combination with the remote transmitter SAB3011 in microcomputer controlled tuning concepts.
- High security against interferences by word format checking and double word testing, also in case of a simultaneous infrared sound transmission.
- Asynchronous serial command output to the microcomputer with processing of acknowledgement signals produced by the microcomputer.
- Relieving the microcomputer of real time processing, e.g. incoming signals are permanently checked with the command format validity and freedom from interferences.
- Separate inputs for local operation (up to 31 commands); mask-programmable.
- Only three terminals of the microcomputer are necessary for the control part of the television receiver.
- Internal clock oscillator.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Oscillator frequency	f_{QRZ}	typ.	4 MHz
Supply current; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	typ.	20 mA

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

GENERAL DESCRIPTION

The SAB3042 decodes the pulse code modulated signals from the remote transmitter SAB3011. Correct reception of two command words activates the IBUS outputs $\overline{\text{DLEN}}$ and $\overline{\text{DATA}}$, as well as the CBUS signals $\overline{\text{DAV}}$, $\overline{\text{LINH}}$ and SHCL. The IBUS outputs can be used for driving systems which are accessible via this type of interface, e.g. Teletext and Viewdata. The CBUS output data can be used for control of a microcomputer. For local operation, 5 inputs are available (LOCA to LOCE), via which up to 31 commands can be loaded into the command register.

OPERATION DESCRIPTION

Remote control signal input (RSIGI)

The signals from the remote control transmitter are applied to the RSIGI input, where they are checked and decoded. The instruction bus (IBUS) is then enabled and an output operation takes place. The microcomputer is also warned via $\overline{\text{DAV}}$, that a message is waiting. The response time is about 110 ms.

The following tests are carried out for each signal:

- Control of pulse distance for logic 0 or 1 and word separation.
- Comparison of two successive transmitted words.
- Detection of noise between the signals.

Signals which do not come within the zero or one 'window', restart the timing procedure. The commands are transmitted as 7-bit words (1 start bit, 6 data bits).

Local keyboard inputs (LOCA, LOCB, LOCC, LOCD and LOCE)

The SAB3042 has 5 keyboard inputs for local control. The coding of the commands is initiated via an external diode matrix; up to 31 commands (see Table 1) for local control are possible. The selection of these commands (31 out of 64 available) are stored in a mask-programmable ROM (according to the wishes of the customer).
The inputs are drawn internally to V_{DD}, if the keys are not used.
The response time is 32 ms for local commands.
A local command overrides a remote control command at input RSIGI. The current output data at the IBUS or the CBUS will, however, be completed. For waveforms see Fig. 2.

IBUS outputs ($\overline{\text{DATA}}$, $\overline{\text{DLEN}}$)

Correctly received commands are available for the duration of a key operation as a single command or as repeated commands, in accordance with the sub-system requirements (see Table 1). The following output modes are provided:

- Single command; e.g. digits; instruction class 'S'.
- Repetition rate: 2/second; e.g. step function; instruction class 'R2'.
- Repetition rate: 8/second; e.g. analogue functions; instruction class 'R8'.

The IBUS command is available at output $\overline{\text{DATA}}$ synchronous with the system clock; the word length is 7 bits, one start bit and 6 data bits (see Fig. 3).

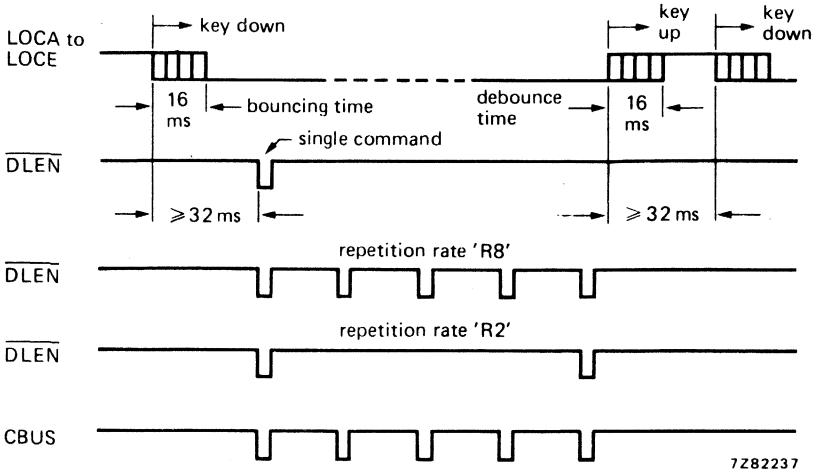


Fig. 2 Relationship between key operation and command output.

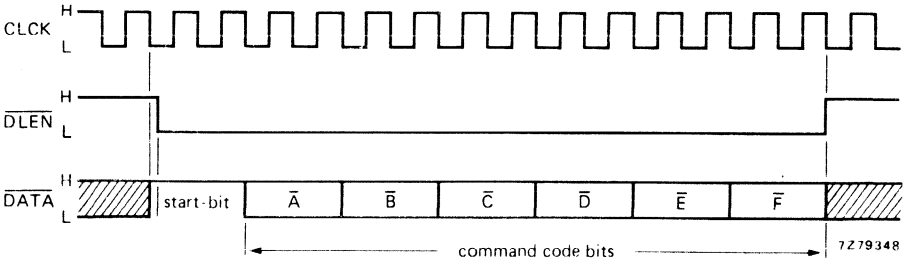


Fig. 3 Output waveforms of a command transmission.

Data output; e.g. request at the CBUS interface

Inputs/outputs ($\overline{DAV}$, $\overline{LINH}$, SHCL)

The CBUS inputs/outputs are assigned for the asynchronous request of a command by external units. The commands activate the CBUS with a repetition rate of 8/second during a key operation. The receiving of a command will be indicated by setting the $\overline{DAV}$ signal to LOW (see Fig. 5). The output will be delayed in case of an occupied BUS ($\overline{DAV}$ = LOW or $\overline{LINH}$ = LOW). Input $\overline{DAV}$ is an input for this control. If the external unit recognizes $\overline{DAV}$ = LOW the request for information is started by setting $\overline{LINH}$ to LOW. The SAB3042 indicates the reception $\overline{LINH}$ = LOW by setting $\overline{DAV}$ to HIGH. The data word can be shifted out after a certain hold time by a series of clock pulses, the frequency of which can be chosen in a wide range. The SAB3042 generates $\overline{DAV}$ = HIGH by applying further clock pulses, after the data word is shifted out.
The request will be terminated by setting $\overline{LINH}$ = HIGH, also in case the data word is not completely shifted out.

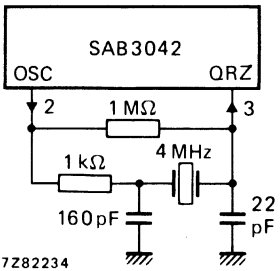
A new incoming command can overrule an enclosed command for as long as the request is not yet started ($\overline{LINH}$ = HIGH). A command, which is overruled, is lost. A stored command cannot be overruled when $\overline{LINH}$ is set LOW.

The following information is shifted out at the CBUS in addition to the 7-bit information of the remote transmitter (start bit S and data bits A to F).

L-bit: this bit indicates, whether the command has been initiated by the local control inputs LOCA to LOCE (L = HIGH), or by the remote control (L = LOW).

R-bit: this bit indicates, whether the previous command is still applied without interruption of the key operation. R is LOW in case the command is on the CBUS output for the first time; R is HIGH for all following commands. The R-bit enables the external system to execute commands as single commands or repeated commands.

Oscillator inputs (OSC, QRZ)

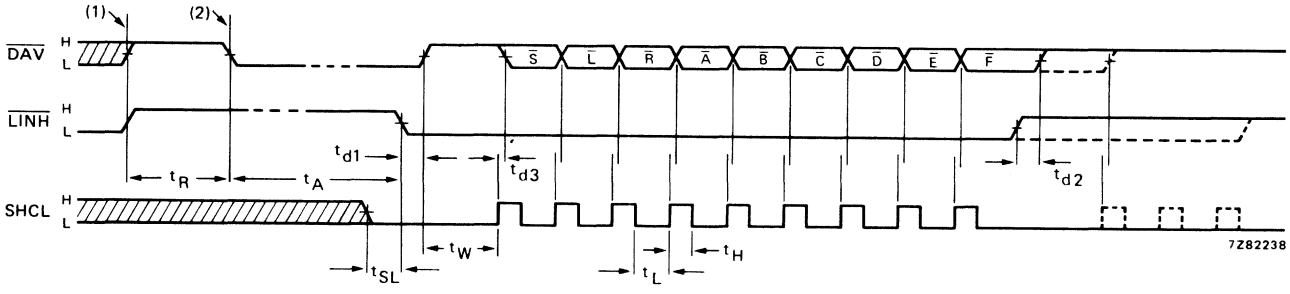


The system clock frequency of 62,5 kHz is generated internally from a 4 MHz quartz crystal oscillator. The terminals QRZ and OSC are the input/output of the 4 MHz oscillator. An external oscillator signal of 4 MHz can be applied to terminal QRZ.

Fig. 4 Application advice for the oscillator.

Reset

The circuit generates a reset signal internally. A reset-cycle with a duration of two clock cycles is automatically initiated after switching on the supply. The IBUS outputs $\overline{DATA}$, $\overline{DLEN}$ and the CBUS output $\overline{DAV}$ are then HIGH.



(1) CBUS is occupied by previous transmission.

(2) Start of a new CBUS transmission by a HIGH-to-LOW transition at output $\overline{DAV}$.

Fig. 5 Waveforms showing CBUS output signals.

Table 1. Specifications of the IBUS/CBUS-code (continued on next page)

RSIGI/ IBUS code no.	local control inputs *					$\overline{DATA}/\overline{DAV}$ output code							IBUS instr. class **
	LOCE	LOCD	LOCC	LOCB	LOCA	S	F	E	D	C	B	A	
0	1	1	0	0	0	0	0	0	0	0	0	0	S
1	0	0	0	0	1	0	0	0	0	0	0	1	S
2	1	1	1	1	0	0	0	0	0	0	1	0	S
3	1	1	1	0	1	0	0	0	0	0	1	1	S
4	0	0	0	1	0	0	0	0	0	1	0	0	R8
5	1	1	0	1	1	0	0	0	0	1	0	1	S
6						0	0	0	0	1	1	0	S
7						0	0	0	0	1	1	1	S
8						0	0	0	1	0	0	0	R8
9						0	0	0	1	0	0	1	R8
10						0	0	0	1	0	1	0	R8
11	0	0	1	0	0	0	0	0	1	0	1	1	R8
12						0	0	0	1	1	0	0	R8
13						0	0	0	1	1	0	1	R8
14						0	0	0	1	1	1	0	R8
15	0	1	0	0	0	0	0	0	1	1	1	1	R8
16	0	0	0	1	1	0	0	1	0	0	0	0	S
17	1	0	1	1	1	0	0	1	0	0	0	1	S
18	0	0	1	0	1	0	0	1	0	0	1	0	S
19	0	0	1	1	0	0	0	1	0	0	1	1	S
20	0	1	0	0	1	0	0	1	0	1	0	0	S
21	0	1	0	1	0	0	0	1	0	1	0	1	S
22	0	1	1	0	0	0	0	1	0	1	1	0	S
23	1	0	0	0	1	0	0	1	0	1	1	1	S
24	1	0	0	1	0	0	0	1	1	0	0	0	S
25	1	0	1	0	0	0	0	1	1	0	0	1	S
26	0	1	1	1	0	0	0	1	1	0	1	0	S
27	0	1	1	0	1	0	0	1	1	0	1	1	S
28						0	0	1	1	1	0	0	S
29	0	1	0	1	1	0	0	1	1	1	0	1	S
30						0	0	1	1	1	1	0	S
31						0	0	1	1	1	1	1	S

* | See next page
** |

RSIGI/ IBUS code no.	local control inputs *					$\overline{DATA}/\overline{DAV}$ output code							IBUS instr. class **
	LOCE	LOCD	LOCC	LOCB	LOCA	S	F	E	D	C	B	A	
32						0	1	0	0	0	0	0	S
33	0	0	1	1	1	0	1	0	0	0	0	1	S
34	1	0	0	1	1	0	1	0	0	0	1	0	S
35						0	1	0	0	0	1	1	S
36	1	0	1	0	1	0	1	0	0	1	0	0	R2
37	1	0	1	1	0	0	1	0	0	1	0	1	R2
38						0	1	0	0	1	1	0	R2
39	1	1	1	0	0	0	1	0	0	1	1	1	R2
40	1	1	0	0	1	0	1	0	1	0	0	0	R8
41	1	1	0	1	0	0	1	0	1	0	0	1	R8
42						0	1	0	1	0	1	0	R8
43						0	1	0	1	0	1	1	R8
44						0	1	0	1	1	0	0	R8
45						0	1	0	1	1	0	1	R8
46						0	1	0	1	1	1	0	R8
47						0	1	0	1	1	1	1	R8
48						0	1	1	0	0	0	0	S
49						0	1	1	0	0	0	1	S
50	0	1	1	1	1	0	1	1	0	0	1	0	S
51						0	1	1	0	0	1	1	S
52						0	1	1	0	1	0	0	R8
53						0	1	1	0	1	0	1	R8
54						0	1	1	0	1	1	0	R8
55						0	1	1	0	1	1	1	R8
56	1	0	0	0	0	0	1	1	1	0	0	0	R8
57	0	0	0	0	0	0	1	1	1	0	0	1	R8
58						0	1	1	1	0	1	0	R8
59						0	1	1	1	0	1	1	R8
60						0	1	1	1	1	0	0	R8
61						0	1	1	1	1	0	1	R8
62						0	1	1	1	1	1	0	R8
63						0	1	1	1	1	1	1	R8
64-127						1	–	–	–	–	–	–	S

* The selection of local commands is mask-programmable. The table gives local commands for the standard version SAB3042B.

** Instruction class: S = single
R2 = repeat ≈ 2/second
R8 = repeat ≈ 8/second.

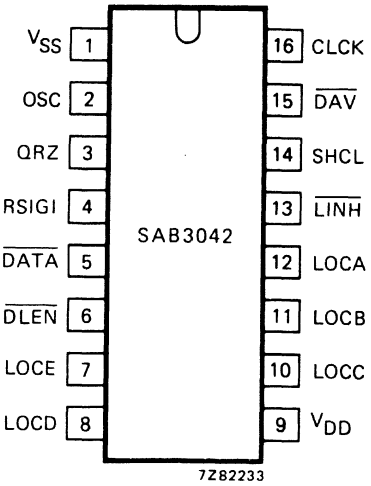


Fig. 6 Pinning diagram.

PINNING

1	V_{SS}	negative supply (0 V)	
9	V_{DD}	positive supply	
4	RSIGI	data input; remote control	
12	LOCA	local keyboard inputs (5-bits)	
11	LOCB		
10	LOCC		
8	LOCD		
7	LOCE		
6	$\overline{DLEN}$	data line enable input/output	IBUS
5	$\overline{DATA}$	data output	
16	CLCK	clock output (62,5 kHz)	
14	SHCL	asynchronous clock-burst	CBUS
15	$\overline{DAV}$	data output	
13	$\overline{LINH}$	control signal	
3	QRZ	oscillator input	
2	OSC	oscillator output	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 7,5	V
Input voltage range	V_I	−0,3 to + 15	V
Input current	$\pm I_I$	max. 10	mA
Output current	$\pm I_O$	max. 10	mA
Power dissipation per output	P_O	max. 50	mW
Total power dissipation per package	P_{tot}	max. 800	mW
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{DD}	4,5	5,0	5,5	V	
Supply current	5	I_{DD}	–	–	25	mA	
Inputs RSIGI, $\overline{\text{LINH}}$, QRZ, LOCA to LOCE							
Input voltage LOW	5	V_{IL}	−0,3	–	1,2	V	
Input voltage HIGH	5	V_{IH}	2,0	–	15	V	
Input leakage current	5	I_{IR}	–	–	1	μA	V_I = −0,3 to + 15 V
Input current LOW LOCA to LOCE	5	$-I_{IL}$	10	–	100	μA	V_I = 0
Outputs $\overline{\text{DATA}}$, $\overline{\text{DAV}}$, OSC (open drain)							
Output leakage current	5	I_{QR}	–	–	20	μA	V_Q = 15 V
Output voltage LOW $\overline{\text{DATA}}$	5	V_{QL}	–	–	1	V	$-I_Q$ = 1 mA
$\overline{\text{DAV}}$, OSC	5	V_{QL}	–	–	0,4	V	$-I_Q$ = 1,6 mA
Input/output $\overline{\text{DLEN}}$ (open drain)							internal high-ohmic pull-up transistor
Input values	–	–	see RSIGI				
Output values	–	–	see $\overline{\text{DATA}}$				
Input current LOW	5	$-I_{IL}$	10	–	100	μA	V_I = 0
Input/output CLCK							
Input values	–	–	see RSIGI				
Input current LOW	5	$-I_{IL}$	10	–	100	μA	V_I = 0
Output voltage LOW	5	V_{QL}	–	–	1	V	$-I_Q$ = 5 mA
Output leakage current	5	I_{QR}	–	–	20	μA	V_Q = 15 V

CHARACTERISTICS (continued)

	V_{DD} V	symbol	min.	typ.	max.		conditions
Oscillator frequency QRZ, OSC	5	f	3	4	4,1	MHz	
Duty factor	5	δ	0,4	0,5	0,6		
Switching times see Fig. 5	5	t_R	1	–	4	ms	f_{QRZ} = 4 MHz
	5	t_{d1}; t_{d2}	–	–	20	μs	f_{QRZ} = 4 MHz
	5	t_{d3}	–	–	5	μs	
	5	t_A	0	–	–	μs	
	5	t_{SL}; t_W; t_H; t_L	5	–	–	μs	
Input rise/fall times							
Input QRZ	5	t_r; t_f	–	–	50	ns	
All other inputs	5	t_r; t_f	–	–	1	μs	

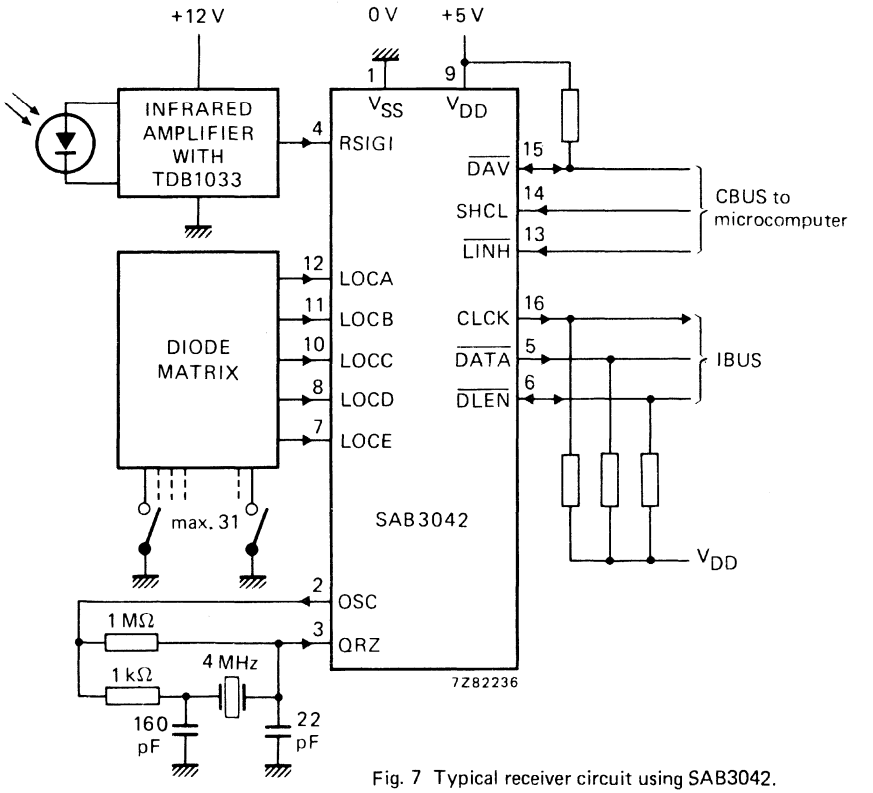


Fig. 7 Typical receiver circuit using SAB3042.

REMOTE CONTROL SYSTEM FOR INFRARED OPERATION

The SAF1032P (receiver/decoder) and the SAF1039P (transmitter) form the basic parts of a sophisticated remote control system (pcm: pulse code modulation) for infrared operation. The ICs can be used, for example, in TV, audio, industrial equipment, etc.

Features:

SAF1032P receiver/decoder:

- 16 programme selection codes
- automatic preset to stand-by at power 'ON', including automatic analogue base settings to 50% and automatic preset of programme selection '1' code
- 3 analogue function controls, each with 63 steps
- single supply voltage
- protection against corrupt codes.

SAF1039P transmitter:

- 32 different control commands
- static keyboard matrix
- current drains from battery only during key closure time
- two transmission modes selectable.

The devices are implemented in LOCMOS (Local Oxidation Complementary MOS) technology to achieve an extremely low power consumption.

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

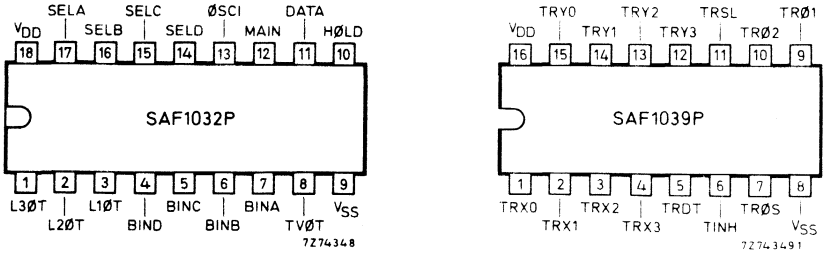


Fig. 1 Pin designations.

PACKAGE OUTLINES

SAF1032P: 18-lead DIL; plastic (SOT-102A).
SAF1039P: 16-lead DIL; plastic (SOT-38Z).

PINNING

To facilitate easy function recognition, each integrated circuit pin has been allocated a code as shown below.

SAF1032P

1	L3ØT	linear output	10	HØLD	control input
2	L2ØT	linear output	11	DATA	data input
3	L1ØT	linear output	12	MAIN	reset input
4	BIND	binary 8 output	13	ØSCI	clock input
5	BINC	binary 4 output	14	SELD	binary 8 output
6	BINB	binary 2 output	15	SELC	binary 4 output
7	BINA	binary 1 output	16	SELB	binary 2 output
8	TVØT	on/off input/output	17	SELA	binary 1 output
9	V_{SS}		18	V_{DD}	

SAF1039P

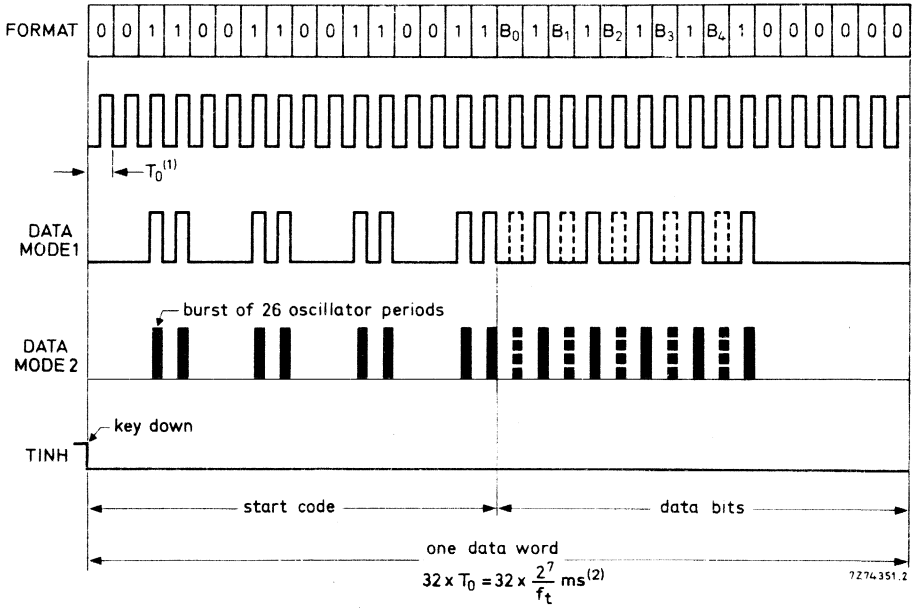
1	TRX0	keyboard input	9	TRØ1	oscillator control input
2	TRX1	keyboard input	10	TRØ2	oscillator control input
3	TRX2	keyboard input	11	TRSL	keyboard select line
4	TRX3	keyboard input	12	TRY3	keyboard input
5	TRDT	data output	13	TRY2	keyboard input
6	TINH	inhibit output/mode select input	14	TRY1	keyboard input
7	TRØS	oscillator output	15	TRY0	keyboard input
8	V_{SS}		16	V_{DD}	

BASIC OPERATING PRINCIPLES

The data to be transmitted are arranged as serial information with a fixed pattern (see Fig. 2), in which the data bit-locations B_0 to B_4 represent the generated key-command code. To cope with IR (infrared) interferences of other sources a selective data transmission is present. Each transmitted bit has a burst of 26 oscillator periods.

Before any operation will be executed in the receiver/decoder chip, the transmitted data must be accepted twice in sequence. This means the start code must be recognized each time a data word is applied and comparison must be true between the data bits of two successively received data words. If both requirements are met, one group of binary output buffers will be loaded with a code defined by the stored data bits, and an internal operation can also take place. See operating code table on page 7.

The contents of the 3 analogue function registers are available on the three outputs in a pulse code versus time modulation format after D (digital) to A (analogue) conversion. The proper analogue levels can be obtained by using simple integrated networks. For local control a second transmitter chip (SAF1039P) is used (see Fig. 7).



(1) T_0 = 1 clock period = 128 oscillator periods. (2) f_t in kHz.

Fig. 2 Pattern for data to be transmitted.

TIMING CONSIDERATIONS

The transmitter and receiver operate at different oscillator frequencies. Due to the design neither frequency is very critical, but correlation between them must exist. Calculation of these timing requirements shows the following.

With a tolerance of ±10% on the oscillator frequency (f_t) of the transmitter, the receiver oscillator frequency ($f_r = 3 \times f_t$) must be kept constant with a tolerance of ±20%.
On the other hand, the data pulse generated by the pulse stretcher circuit (at the receiver side) may vary ±25% in duration.

GENERAL DESCRIPTION OF THE SAF1039P TRANSMITTER

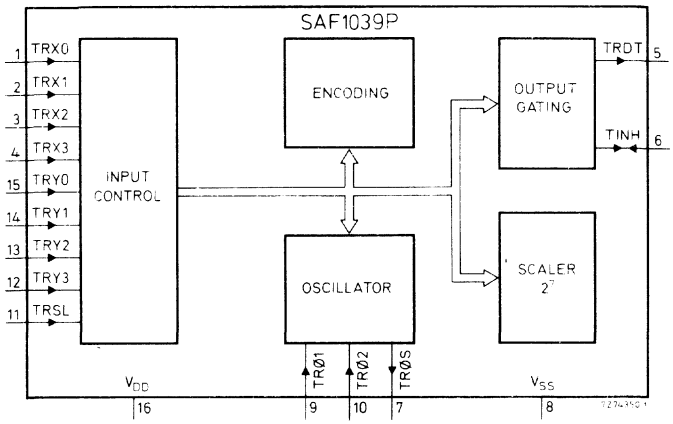


Fig. 3 Block diagram of SAF1039P transmitter.

Any keyboard activity on the inputs TRX0 to TRX3, TRY0 to TRY3 and TRSL will be detected. For a legal key depression, one key down at a time (one TRX and TRY input activated), the oscillator starts running and a data word, as shown on page 3, is generated and supplied to the output TRDT. If none, or more than 2 inputs are activated at the same time, the input detection logic of the chip will generate an overall reset and the oscillator stops running (no legal key operation).

This means that for each key-bounce the logic will be reset, and by releasing a key the transmitted data are stopped at once.

The minimum key contact time required is the duration of two data words. The on-chip oscillator is frequency controlled with the external components R1 and C1 (see circuit Fig. 6); the addition of resistor R2 means that the oscillator frequency is practically independent of supply voltage variations. A complete data word is arranged as shown in Fig. 2, and has a length of 32 x T_0 ms, where $T_0 = 2^7/f_t$.

Operation mode

	DATA	FUNCTION OF TINH
1	unmodulated: LOCAL operation	output, external pull-up resistor to V_{DD}
2	modulated: REMOTE control	input, connected to V_{SS}

GENERAL DESCRIPTION OF THE SAF1032P RECEIVER/DECODER

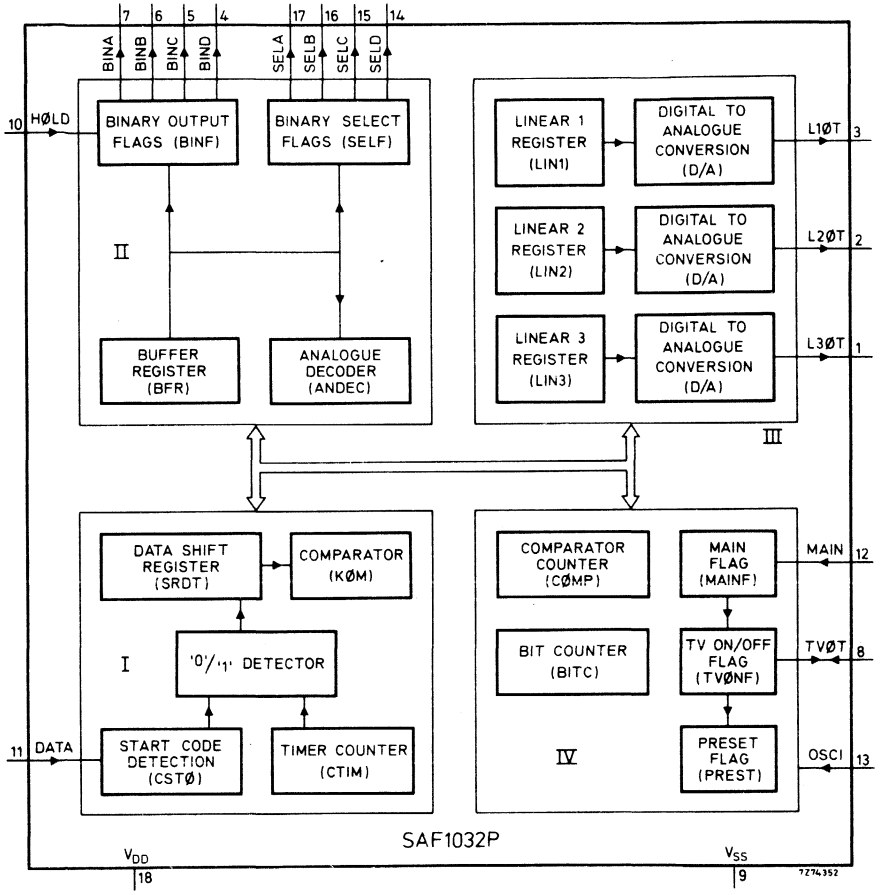


Fig. 4 Block diagram of SAF1032P receiver/decoder.

The logic circuitry of the receiver/decoder chip is divided into four main parts as shown in the block diagram above.

Part I

This part decodes the applied DATA information into logic '1' and '0'.
It also recognizes the start code and compares the stored data-bits with the new data-bits accepted.

Part II

This part stores the programme selection code in the output group (BINF) and memorizes it for condition HØLD = LOW.

It puts the functional code to output group (SELF) during data accept time, and decodes the internally used analogue commands (ANDEC).

Part III

This part controls the analogue function registers (each 6-bits long), and connects the contents of the three registers to the analogue outputs by means of D/A conversion. During sound mute, output L1ØT will be forced to HIGH level.

Part IV

This part keeps track for correct power 'ON' operation, and puts chip in 'stand-by' condition at supply voltage interruptions.

The logic design is dynamic and synchronous with the clock frequency (ØSCI), while the required control timing signals are derived from the bit counter (BITC).

Operation

Serial information applied to the DATA input will be translated into logic '1' and '0' by means of a time ratio detector.

After recognizing the start code (CSTØ) of the data word, the data bits will be loaded into the data shift register (SRDT). At the first trailing edge of the following data word a comparison (KØM) takes place between the contents of SRDT and the buffer register (BFR). If SRDT equals BFR, the required operation will be executed under control of the comparator counter (CØMP).

As shown in the operating code table on page 7, the 4-bit wide binary output buffer (BINF) will be loaded for BFR0 = '0', while for BFR0 = '1' the binary output buffer (SELF), also 4-bit wide will be activated during the data accept time.

At the same time operations involving the internal commands are executed. The contents of the analogue function registers (each 6-bits long) are controlled over 63 steps, with minimum and maximum detection, while the D/A conversion results in a pulsed output signal with a conversion period of 384 clock periods (see Fig. 5).

First power 'ON' will always put the chip in the 'stand-by' position. This results in an internal clearing of all logic circuitry and a 50% presetting of the contents of the analogue registers (analogue base value). The programme selection '1' code will also be prepared and all the outputs will be non-active (see table on page 8).

From 'stand-by' the chip can be made operational via a programme selection command, generated LOCAL or via REMOTE, or directly by forcing the TV ON/OFF output (TVØT) to zero for at least 2 clock periods of the oscillator frequency.

For POWER ON RESET a negative-going pulse should be applied to input MAIN, when V_{DD} is stabilized; pulse width LOW $\geqslant$ 100 μs.

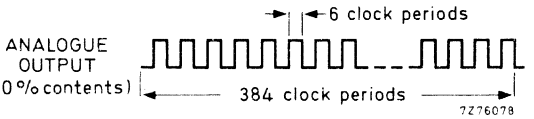


Fig. 5 Analogue output pulses.

OPERATING CODE TABLE

key-matrix position			buffer BFR					BINF (BIN.)				SELF (SEL.)				function
TRX.	TRY.	TRSL	0	1	2	3	4	A	B	C	D	A	B	C	D	
0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	programme select + ON
0	1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	
0	2	0	0	0	1	0	0	0	1	0	0	1	1	1	1	
0	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	
1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	
1	1	0	0	1	0	1	0	1	0	1	0	1	1	1	1	
1	2	0	0	1	1	0	0	0	1	1	0	1	1	1	1	
1	3	0	0	1	0	0	0	1	1	1	0	1	1	1	1	
2	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	programme select + ON
2	1	0	0	0	0	1	1	1	0	0	1	1	1	1	1	
2	2	0	0	0	1	0	1	0	1	0	1	1	1	1	1	
2	3	0	0	0	0	0	1	1	1	0	1	1	1	1	1	
3	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1	
3	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	
3	2	0	0	1	1	0	1	0	1	1	1	1	1	1	1	
3	3	0	0	1	0	0	1	1	1	1	1	1	1	1	1	
0	0	1	1	0	1	1	0	X	X	X	X	0	1	1	1	analogue base
0	1	1	1	0	0	1	0	X	X	X	X	0	0	1	1	reg. (LIN3) + 1
0	2	1	1	0	1	0	0	X	X	X	X	0	1	0	1	reg. (LIN2) + 1
0	3	1	1	0	0	0	0	X	X	X	X	0	0	0	1	reg. (LIN1) + 1
1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	OFF
1	1	1	1	1	0	1	0	X	X	X	X	1	0	1	1	reg. (LIN3) − 1
1	2	1	1	1	1	0	0	X	X	X	X	1	1	0	1	reg. (LIN2) − 1
1	3	1	1	1	0	0	0	X	X	X	X	1	0	0	1	reg. (LIN1) − 1
2	0	1	1	0	1	1	1	X	X	X	X	0	1	1	0	mute (set/reset)
2	1	1	1	0	0	1	1	X	X	X	X	0	0	1	0	spare functions
2	2	1	1	0	1	0	1	X	X	X	X	0	1	0	0	
2	3	1	1	0	0	0	1	X	X	X	X	0	0	0	0	
3	0	1	1	1	1	1	1	X	X	X	X	1	1	1	0	
3	1	1	1	1	0	1	1	X	X	X	X	1	0	1	0	
3	2	1	1	1	1	0	1	X	X	X	X	1	1	0	0	
3	3	1	1	1	0	0	1	X	X	X	X	1	0	0	0	

Note

Reset mute also on programme select codes, (LIN1) ± 1, and analogue base.

OPERATING OUTPUT CODE

	(BIN.)				(SEL.)				(LØT)			TVØT
	A	B	C	D	A	B	C	D	1	2	3	
'stand-by' OFF via remote	0	0	0	0	0	0	0	0	1	0	0	1
ON → 'not hold' condition non-operating	1	1	1	1	1	1	1	1	X	X	X	0
ON — 'hold' condition non-operating	X	X	X	X	1	1	1	1	X	X	X	0

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}-V_{SS}		−0,5 to 11	V
Input voltage	V_I	max.	11	V
Current into any terminal	$\pm I_I$	max.	10	mA
Power dissipation (per output)	P_o	max.	50	mW
Power dissipation (per package)	P_{tot}	max.	200	mW
Operating ambient temperature	T_{amb}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1039P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	7	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	10	μA	10	25
		–	1	50	μA	7	65
operating; TRØ1 at V_{SS}; outputs unloaded; one keyboard switch closed	I_{DD}	–	–	1,7	mA	10	all
		–	0,8	–	mA	10	25
Inputs (note 1)							
TRØ2; TINH (note 2)							
input voltage HIGH	V_{IH}	$0,8V_{DD}$	–	V_{DD}	V	7 to 10	all
input voltage LOW	V_{IL}	0	–	$0,2V_{DD}$	V	7 to 10	all
input current	I_I	–	10^{-5}	1	μA	10	25
Outputs							
TRDT; TRØS; TRØ1							
output current HIGH at $V_{OH} = V_{DD} - 0,5$ V	$-I_{OH}$	0,4	–	–	mA	7	all
output current LOW at V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
TRDT output leakage current when disabled $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	1	μA	10	25
TINH							
output current LOW V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
Oscillator							
frequency variation with supply voltage, temperature and spread of IC properties f_{nom} = 36 kHz (note 3)	Δf	–	–	$0,15f_{nom}$		7 to 10	all
oscillator current drain	I_{osc}	–	–	2,5	mA	10	all
		–	1,3	–	mA	10	25

For notes see page 11.

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1032P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	8	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	50	μA	10	25
		–	1	300	μA	10	85
operating; I_O = 0; at ØSCI frequency of 100 kHz	I_{DD}	–	–	1	mA	10	all
Inputs							
DATA; ØSCI; HØLD; TVØT (see note 4)							
input voltage HIGH	V_{IH}	0,7V_{DD}	–	V_{DD}	V	8 to 10	all
input voltage LOW	V_{IL}	0	–	0,2V_{DD}	V	8 to 10	all
MAIN; tripping levels							
input voltage increasing	V_{ti}	0,4V_{DD}	–	0,9V_{DD}	V	5 to 10	all
input voltage decreasing	V_{td}	0,1V_{DD}	–	0,6V_{DD}	V	5 to 10	all
input current; all inputs except TVØT	I_I	–	10^{-5}	1	μA	10	25
input signal rise and fall times (10% and 90% V_{DD}) all inputs except MAIN	t_r, t_f	–	–	5	μs	8 to 10	all
Outputs							
programme selection: BINA/B/C/D							
auxiliary: SELA/B/C/D							
analogue: L3ØT; L2ØT; L1ØT TVØT (note 4)							
all open drain n-channel							
output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA	8	all
output leakage current at V_O = V_{SS} to V_{DD}	I_{OL}	–	–	10	μA	10	all

For note 4 see page 11.

Notes (to pages 9 and 10)

1. The keyboard inputs (TRX.; TRY.; TRSL) are not voltage driven (see application information diagram Fig. 6).

   If one key is depressed, the circuit generates the corresponding code. The number of keys depressed at a time, and this being recognized by the circuit as an illegal operation, depends on the supply voltage (V_{DD}) and the leakage current (between device and printed-circuit board) externally applied to the keyboard inputs.

   If no leakage is assumed, the circuit recognizes an operation as illegal for any number of keys > 1 depressed at the same time with $V_{DD} = 7$ V. At a leakage due to a 1 MΩ resistor connected to each keyboard input and returned to either V_{DD} or V_{SS}, the circuit recognizes at least 2 keys depressed at a time with $V_{DD} = 7$ V.

   The highest permissible values of the contact series resistance of the keyboard switches is 500 Ω.

2. Inhibit output transistor disabled.

3. Δf is the width of the distribution curve at 2 σ points (σ = standard deviation).

4. Terminal TVØT is input for manual 'ON'. When applying a LOW level TVØT becomes an output carrying a LOW level.

APPLICATION INFORMATION

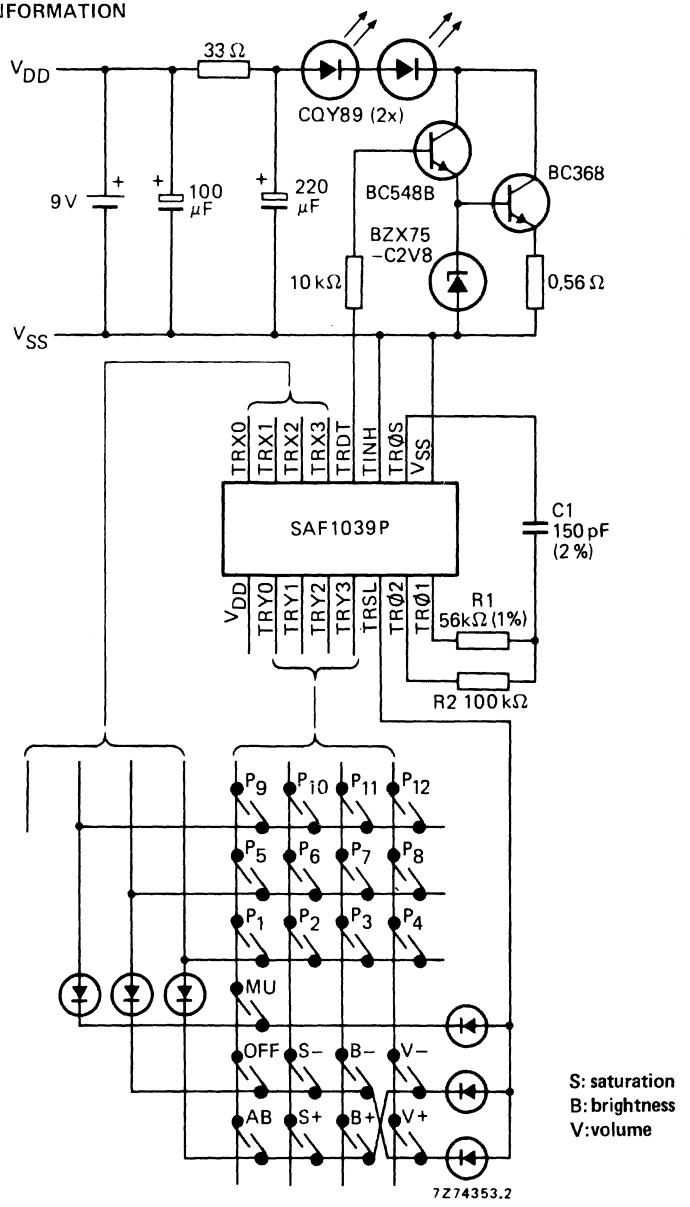


Fig. 6 Interconnection diagram of transmitter circuit SAF1039P in a remote control system, for a television receiver with 12 programmes.

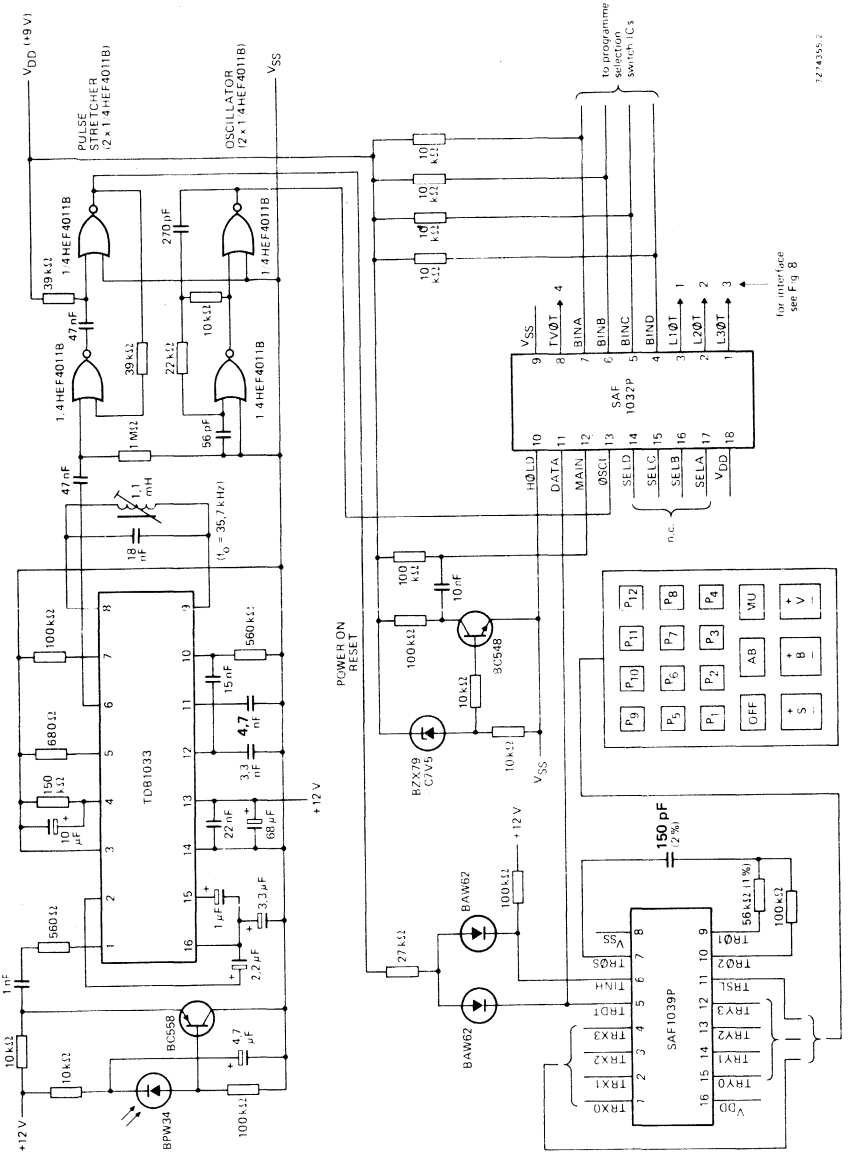


Fig. 7 Interconnection diagram showing the SAF1032P and SAF1039P used in a TV control system.

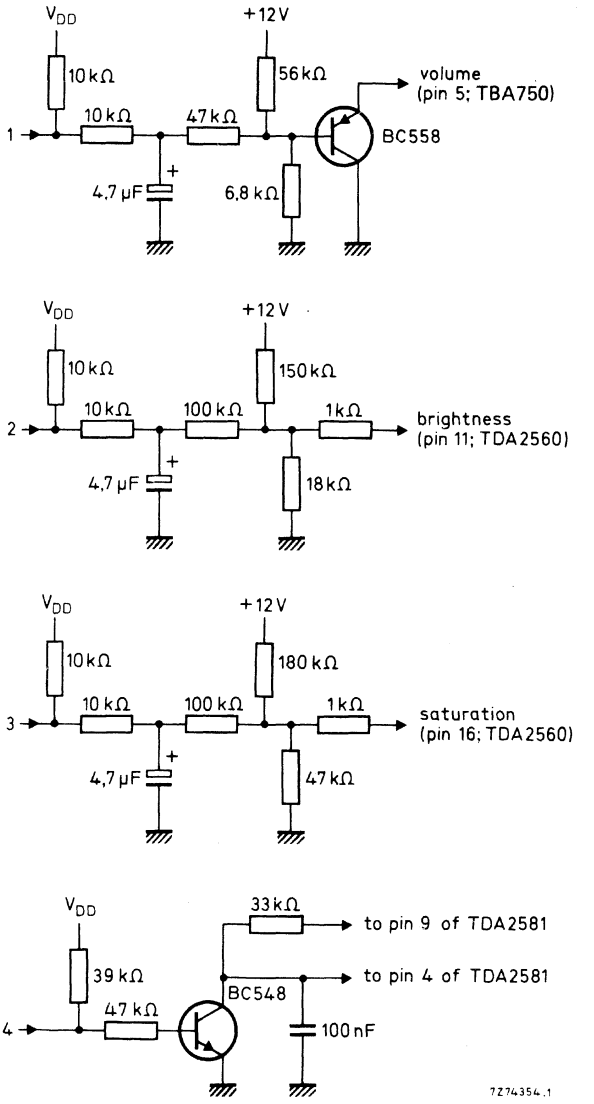


Fig. 8 Additional circuits from outputs L1ØT (1), L2ØT (2), L3ØT (3) and TVØT (4) of the SAF1032P in circuit of Fig. 7.

PREAMPLIFIER FOR ULTRASONIC/INFRARED REMOTE CONTROL TRANSMISSION

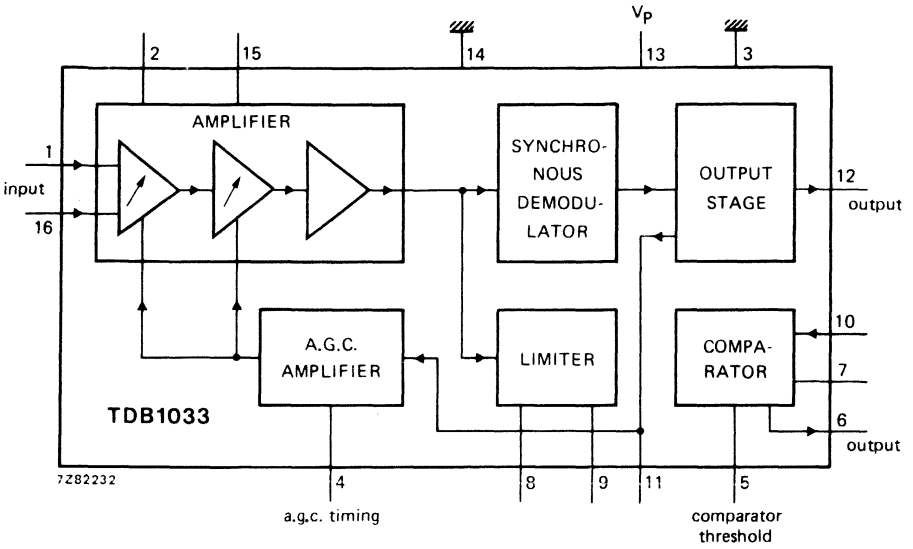


Fig. 1 Block diagram.

Features

- Three differential amplifier stages; two of which are gain controlled.
- The a.g.c. time-constant can be determined externally.
- Built-in synchronous demodulator with limiter and a.g.c. amplifier.
- Comparator for improving the noise performance, with adjustable threshold.

QUICK REFERENCE DATA

Supply voltage	V_P	typ.	12 V
Voltage gain	G_v	typ.	97 dB
Input sensitivity (r.m.s. value)	$V_{i(rms)}$	typ.	110 μV
Supply current	I_P	typ.	38 mA
Operating ambient temperature range	T_{amb}		−20 to +60 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

GENERAL DESCRIPTION

The TDB1033 comprises 3 differential amplifier stages, of which the first and second stages are gain controlled. The output of the third stage is connected to a synchronous demodulator and limiter (reference signal for switching the demodulator). The demodulator is followed by an output stage which delivers a positive-going and a negative-going output signal. The negative-going signal is used to obtain the a.g.c. signal.
The a.g.c. time-constant can be determined by an external RC circuit. The output stage signal is externally connected to the input of the comparator, of which the threshold voltage can be adjusted by choice of an external resistor.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	$V_P = V_{13-3}$	max.	15 V
Input voltage	$V_I = V_{16-1}$	max.	V_P
Input current	$I_I = I_{16/1}$	max.	2 mA
Total power dissipation	P_{tot}	max.	600 mW
Operating ambient temperature range	T_{amb}		−20 to +60 °C
Storage temperature range	T_{stg}		−20 to +125 °C

CHARACTERISTICS

$V_P = V_{13} = +12$ V; $V_3 = 0$ (ground); $T_{amb} = 25$ °C; unless otherwise specified

Quiescent current	$I_P = I_{13}$	typ.	38 mA
Input resistance			
symmetrical	R_{16-1}	typ.	18 kΩ
non-symmetrical	$R_{1-3} = R_{16-3}$	typ.	9 kΩ
Output resistance of output stage			
negative-going output	R_{11-3}	typ.	9 kΩ
positive-going output	R_{12-3}	typ.	14 kΩ

Gain control

The control voltage depends on the amplitude, the repetition rate, and the duty factor of the input signal. The control voltage range is 0 to 5,4 V (see Fig. 2)

Output voltages in the control range at $V_I = V_{16-3(rms)} = 1$ mV

LOW level; measured at pin 12	V_{12L}	typ.	0,5 V
HIGH level; measured at pin 12	V_{12H}	typ.	5,5 V
LOW level; measured at pin 11	V_{11L}	typ.	1,2 V
HIGH level; measured at pin 11	V_{11H}	typ.	5,9 V

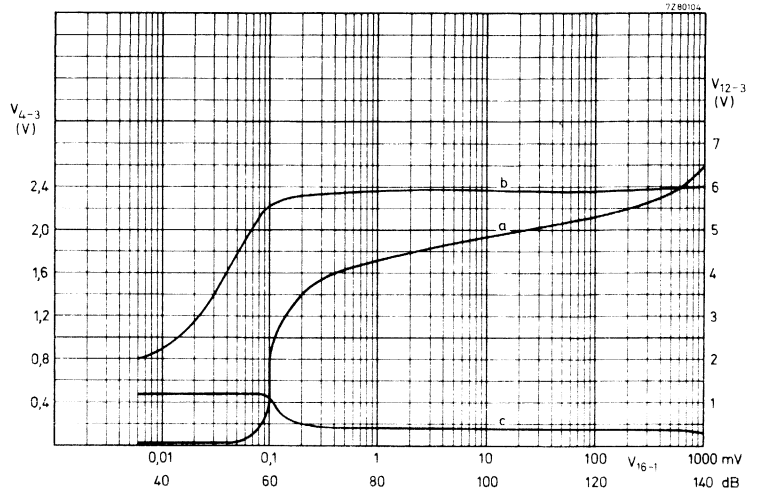


Fig. 2 Typical behaviour of the control voltage V_{4-3} (curve a) and the demodulated output voltage V_{12-3} (HIGH level is curve b; LOW level is curve c) as a function of the r.m.s. input voltage V_{16-1} (measured within the pulse-burst, see Fig. 4).

Comparator

Output voltage without drive	V_{6-3}	typ.	0,7 V
Output voltage with drive	V_{6-3}	typ.	9,2 V
Rate of rise of output voltage	$\Delta V_{6-3}/\Delta t$	>	1,5 V/μs
Rate of fall of output voltage	$\Delta V_{6-3}/\Delta t$	>	1,0 V/μs
Resistance for threshold adjustment (see Fig. 3)	R_{5-3}		1 to 4,7 kΩ
Internal resistance	R_{6-3}	typ.	5 kΩ

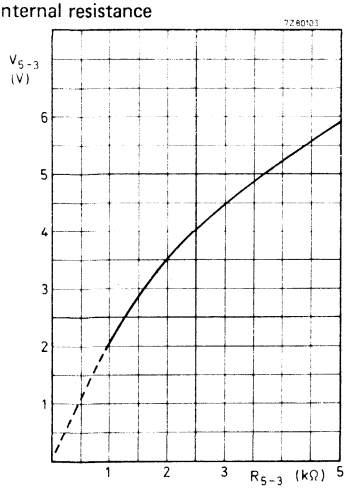


Fig. 3 Typical dependency of the threshold level of the comparator on the resistor value between pins 5 and 3 (ground).

CHARACTERISTICS (continued)

Limiter

D.C. voltage at pins 8 and 9 with respect to ground			typ.	7,3 V
Signal at the LC resonant circuit (peak-to-peak value) at $V_{16\text{-}1(rms)}$ = 1 mV; limiter is active		$V_{8\text{-}9(p\text{-}p)}$	typ.	2,1 V
The TDB1033 used as signal amplifier for infrared transmission (see Fig. 4).				
Input voltage at $R_{5\text{-}3}$ = 1 kΩ		$V_{16\text{-}3}$	typ. <	110 μV 400 μV
D.C. level at pins 12 and 11; $V_{16\text{-}3}$ = 0		$V_{12\text{-}3}$ $V_{11\text{-}3}$	typ. typ.	1 V 5,4 V
Voltage gain with comparator and LC circuit at $R_{5\text{-}3}$ = 1 kΩ	$G_V = 20 \log \frac{V_{6\text{-}3(p\text{-}p)}}{V_{16\text{-}3(rms)}}$		> typ.	88 dB 97 dB
Voltage gain without comparator and with LC circuit	$G_V = 20 \log \frac{V_{12\text{-}3(p\text{-}p)}}{V_{16\text{-}3(p\text{-}p)}}$		> typ.	78 dB 87 dB
Control range at $\Delta V_{12\text{-}3}$ = 2 dB		$\Delta V_{16\text{-}3}$	>	77 dB
Noise voltage at pins 11 and 12 (r.m.s. value) measured with a large bandwidth; $V_{16\text{-}3}$ = 0		$V_{12\text{-}3(rms)}$ $V_{11\text{-}3(rms)}$	typ. typ.	100 mV 100 mV

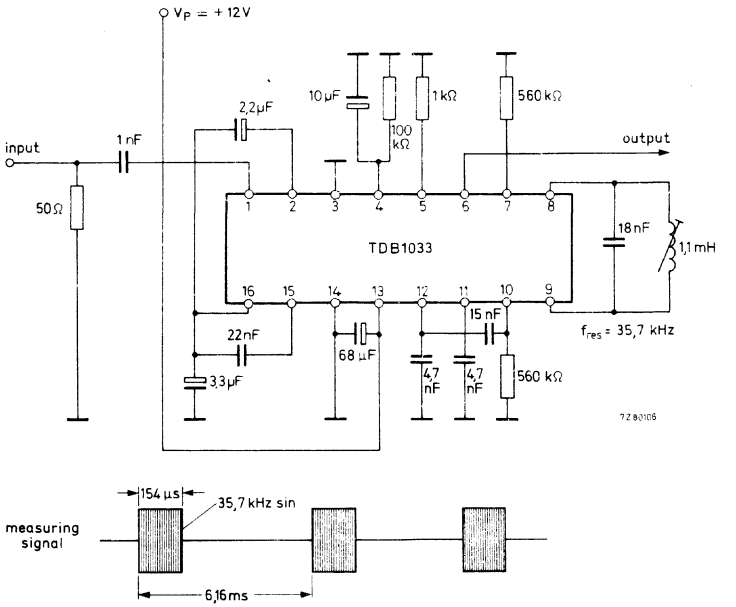
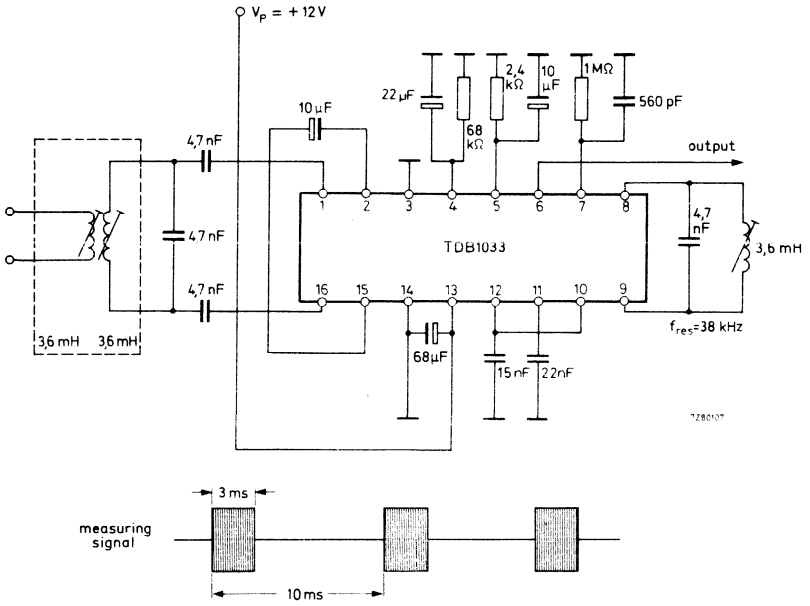


Fig. 4 Measuring circuit for infrared transmission; for coil data see Fig. 6.

The TDB1033 used as signal amplifier for ultrasonic transmission (see Fig. 5).

Input voltage ar R_{5-3} = 2,4 kΩ (r.m.s. value)		$V_{16-3(rms)}$	<	100 μV
D.C. level at pins 12 and 11; $V_{16-3} = 0$		V_{12-3}	typ.	1 V
		V_{11-3}	typ.	5,4 V
Voltage gain with comparator and LC circuit at R_{5-3} = 2,4 kΩ	$G_V = 20 \log \frac{V_{6-3(p-p)}}{V_{16-1(rms)}}$		>	100 dB
Voltage gain without comparator and with LC circuit	$G_V = 20 \log \frac{V_{12-3(p-p)}}{V_{16-1(p-p)}}$		>	90 dB
Control range at ΔV_{12-3} = 1 dB		ΔV_{16-3}	>	65 dB
Noise voltage at pins 11 and 12 (r.m.s. value) measured with a large bandwidth; $V_{16-1} = 0$ V		$V_{12-3(rms)}$	typ.	60 mV
		$V_{11-3(rms)}$	typ.	60 mV



Fif. 5 Measuring circuit for ultrasonic transmission; for coil data see Fig. 9.

APPLICATION INFORMATION

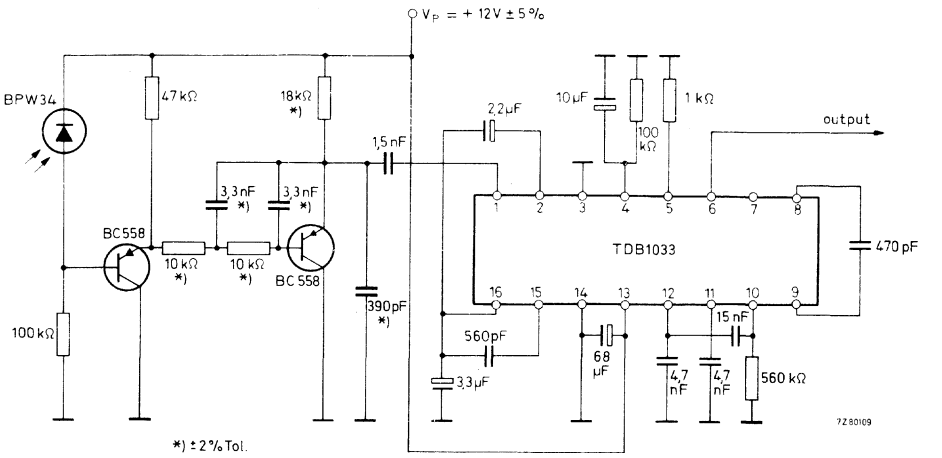


Fig. 6 Preamplifier for infrared transmission with passive double-T suppression filter for 95 kHz and with LC demodulator circuit. Coil data: 240 turns, 0,18 ϕ enamelled copper wire; R = 3,5 Ω; L = 1 mH; frame core and Ferroxcube grade 38 screw core with trimming stud at one end.

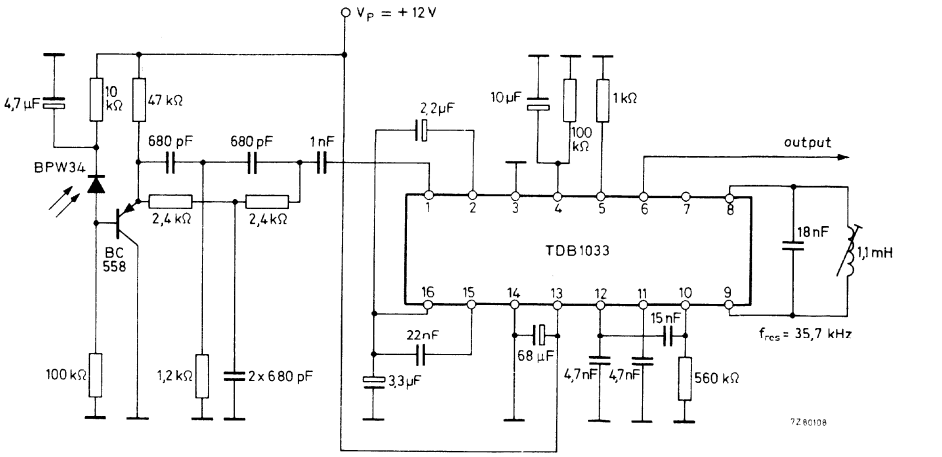


Fig. 7 Preamplifier for infrared transmission with a Chebyshev-filter having a resonance frequency of 35,7 kHz.

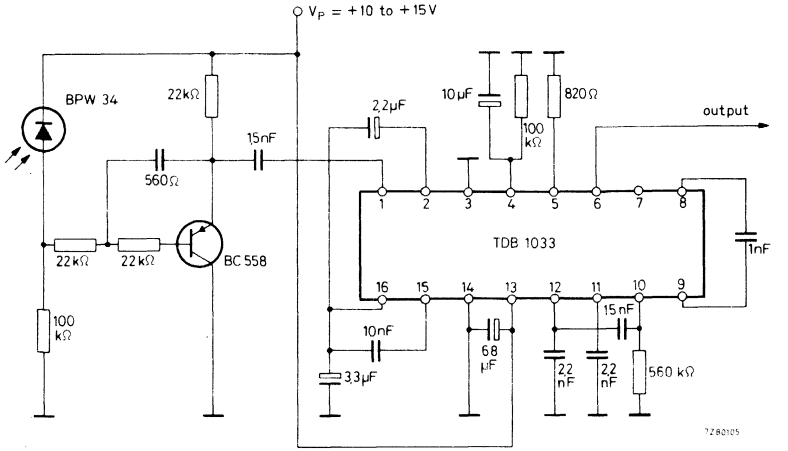


Fig. 8 Simplified preamplifier for infrared transmission with a Butterworth-low-pass filter; angular frequency is 35,7 kHz.

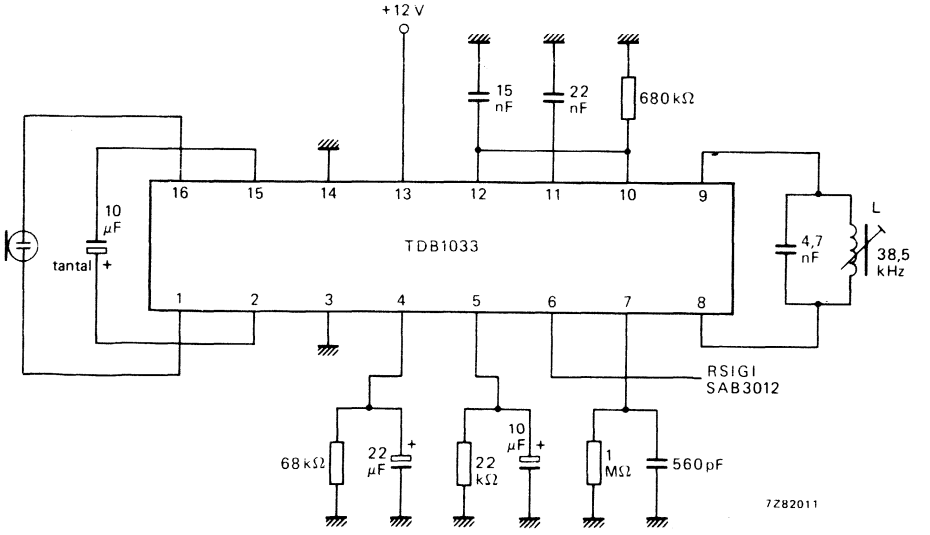


Fig. 9 Preamplifier with ultrasonic transmission with symmetrical PXE transducer. Coil data: 390 turns, 0,12 ϕ enamelled copper wire; R = 12 Ω; L = 3,6 mH; frame core and Ferroxcube grade 3B screw core with trimming stud at one end.

ICs FOR DIGITAL SYSTEMS IN RADIO AND TELEVISION RECEIVERS